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PATENT ABSTRACTS OF JAPAN

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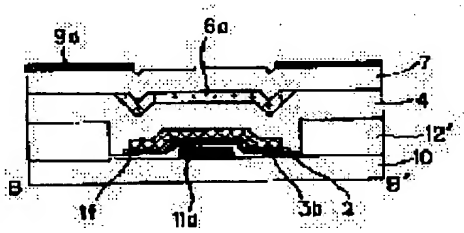
(54) LIQUID CRYSTAL DEVICE AND ITS MANUFACTURE, AND ELECTRONIC EQUIPMENT

(57)Abstract:
PROBLEM TO BE SOLVED: To reduce a defect in alignment of liquid crystal which possibly causes an increase in storage capacity and deterioration in picture quality by recessing an inter-layer insulating film in an area facing a 2nd storage capacity electrode part below at least a data line of a capacity line.
SOLUTION: A 1st inter-layer insulating film 12' formed of a single or more layers is provided between a shading film 11a and pixel switching TFTs. The 1st inter-layer insulating film 12' is formed over the entire surface of a FTF array substrate to function as a substrate film for the pixel switching TFTs. In the area which includes the capacity line 3b formed, specially, below the data line 6a and is encircled with the thick line, the 1st inter-layer insulating film 12' is recessed and formed. Consequently, the alignment defect of liquid crystal can effectively be reduced.



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CLAIMS

[Claim(s)]

[Claim 1] It comes to enclose liquid crystal between the substrates of a couple. The data line of plurality [top / substrate / of the substrate of this couple / one], Two or more scanning lines which intersect two or more of these data lines, and two or more TFT respectively connected to the data line and the scanning line of the aforementioned plurality, Two or more pixel electrodes which were respectively connected to two or more of these TFT, and have been arranged more nearly up than the aforementioned data line, Two or more 1st storage-capacitance polar zone which consisted of the same material as the semiconductor layer which constitutes the drain or source field of two or more of these TFT, and was respectively installed in the bottom of the aforementioned data line at least, Two or more capacity lines which contain respectively the 2nd storage-capacitance polar zone by which opposite arrangement was respectively carried out through the 1st storage-capacitance polar zone and insulator layer of the aforementioned plurality under the aforementioned data line, It has at least one layer insulation film arranged between aforementioned one substrate and the aforementioned pixel electrode. the aforementioned layer insulation film Liquid crystal equipment which the field which counters the aforementioned 2nd storage-capacitance polar zone which is under the aforementioned data line at least among the aforementioned capacity lines is become depressed and formed in a concave, and is characterized by the bird clapper.

[Claim 2] It comes to enclose liquid crystal between the substrates of a couple. The data line of plurality [top / substrate / of the substrate of this couple / one], Two or more scanning lines which intersect two or more of these data lines, and two or more TFT respectively connected to the data line and the scanning line of the aforementioned plurality, Two or more 1st storage-capacitance polar zone which consisted of the same material as two or more pixel electrodes respectively connected to two or more of these TFT, and the semiconductor layer which constitutes the drain or source field of two or more of these TFT, and was respectively installed in the bottom of the aforementioned data line at least, Two or more capacity lines which contain respectively the 2nd storage-capacitance polar zone by which opposite arrangement was respectively carried out through the 1st storage-capacitance polar zone and insulator layer of the aforementioned plurality under the aforementioned data line, The insulator

layer between the 1st layer arranged between aforementioned one substrate and the aforementioned 1st storage-capacitance polar zone, The insulator layer between the 2nd layer arranged between the aforementioned 2nd storage-capacitance polar zone and the aforementioned data line, It has the insulator layer between the 3rd layer arranged between the aforementioned data line and the aforementioned pixel electrode. among insulator layers between the above 1st, the 2nd, and the 3rd layer at least one insulator layer Liquid crystal equipment characterized by becoming depressed and forming in a concave the field which counters the aforementioned 2nd storage-capacitance polar zone which is under the aforementioned data line at least among the aforementioned capacity lines.

[Claim 3] Two or more aforementioned 1st storage-capacitance polar zone is respectively installed in the scanning line of further the aforementioned plurality, and parallel. Opposite arrangement of two or more aforementioned 2nd storage-capacitance polar zone is further carried out through the aforementioned scanning line, the aforementioned 1st storage-capacitance polar zone installed in parallel, and the aforementioned insulator layer for capacity formation. the above -- the liquid crystal equipment according to claim 2 characterized by becoming depressed and forming in a concave the field where one insulator layer counters the aforementioned 2nd storage-capacitance polar zone parallel to the aforementioned scanning line among the aforementioned capacity lines further even if few

[Claim 4] The liquid-crystal equipment according to claim 3 characterized by to be arranged on the aforementioned pixel electrode, to have packed the orientation film by which rubbing processing was carried out in the direction which met the aforementioned capacity line side from the aforementioned scanning-line side to the scanning line and the capacity line of a couple put in order adjacently at the other aforementioned data line, and the scanning line and the capacity line of the aforementioned couple in the one band section in alignment with the aforementioned scanning line, and to have a wrap shading layer further.

[Claim 5] the above -- liquid crystal equipment given in any 1 term of the claims 2-4 characterized by one insulator layer consisting of monolayers even if few

[Claim 6] the above -- liquid crystal equipment given in any 1 term of the claims 2-4 characterized by for one insulator layer consisting of a monolayer portion and a multilayer portion even if few, and considering as the portion to which the aforementioned monolayer portion became depressed in the aforementioned concave, and considering as the portion to which the

aforementioned multilayer portion has not become depressed in the aforementioned concave

[Claim 7] Between the above 1st and the 2nd layer, an insulator layer is liquid crystal equipment given in any 1 term of the claims 2-6 characterized by consisting of respectively a silicon-oxide film or a silicon nitride film.

[Claim 8] It is liquid crystal equipment given in any 1 term of the claims 2-7 which aforementioned one substrate serves as the aforementioned insulator layer between the 1st layer, and are characterized by for the field which counters the aforementioned 2nd storage-capacitance polar zone which at least one side has under the aforementioned data line at least among the aforementioned capacity lines having become depressed in the concave, and forming it among the above 2nd and the insulator layer between the 3rd layer.

[Claim 9] Liquid crystal equipment given in any 1 term of the claims 2-7 characterized by having further the shading film prepared in the position of two or more aforementioned TFT with which the field for channel formation is seen from aforementioned one substrate side at least, and it laps respectively between the aforementioned substrate and the aforementioned insulator layer between the 1st layer.

[Claim 10] The aforementioned shading film contains the 3rd storage-capacitance polar zone prepared in at least one side and the position which counters through the aforementioned insulator layer between the 1st layer among the portion under the aforementioned data line of the aforementioned 1st storage-capacitance polar zone, and the portion parallel to the aforementioned scanning line. The aforementioned insulator layer between the 1st layer is liquid crystal equipment according to claim 9 characterized by becoming depressed and forming the field between the aforementioned 3rd storage-capacitance polar zone and the aforementioned 1st storage-capacitance polar zone in the aforementioned concave.

[Claim 11] The aforementioned shading film is liquid crystal equipment according to claim 9 or 10 characterized by including at least one of Ti, Cr, W, Ta, Mo, and Pd.

[Claim 12] The aforementioned shading film is liquid crystal equipment given in any 1 term of the claims 9-11 characterized by connecting with the constant source of potential.

[Claim 13] The aforementioned insulator layer between the 1st layer is liquid crystal equipment according to claim 12 characterized by being punctured while being become depressed and formed in the aforementioned concave in the position where the aforementioned constant source of potential is connected as the aforementioned shading film.

[Claim 14] The manufacture method of

the liquid-crystal equipment characterized by to have the process which deposits the insulator layer which is the manufacture method of liquid-crystal equipment according to claim 5, and should constitute the aforementioned monolayer, the process which form the resist pattern corresponding to the portion which became depressed in the this deposited insulator layer at the aforementioned concave by the photolithography, and the etching process which form the portion which etched the predetermined time through this resist pattern, and became depressed in the aforementioned concave.

[Claim 15] The manufacture method of the liquid crystal equipment according to claim 6 characterized by providing the following. The process which deposits the 1st insulator layer which should constitute the aforementioned multilayer portion. The process which forms the resist pattern corresponding to the portion which became depressed in the 1st deposited this insulator layer at the aforementioned concave by the photolithography. The etching process which removes the 1st insulator layer of the above corresponding to the portion which etched through this resist pattern and became depressed in the aforementioned concave. The process which deposits the 2nd insulator layer which should constitute the aforementioned monolayer portion and a multilayer portion on the field which removed the 1st insulator layer of the above, and the 1st insulator layer of the above.

[Claim 16] The aforementioned etching process is the manufacture method of the liquid crystal equipment according to claim 13 or 15 characterized by including the wet etching process which forms the side attachment wall of the portion which became depressed in the aforementioned concave in the shape of a taper.

[Claim 17] The manufacture method of liquid crystal equipment given in any 1 term of claims 14-16 characterized by providing the following. The process formed on the aforementioned insulator layer between the 1st layer so that the aforementioned scanning line and a capacity line may be arranged in the aforementioned pixel inter-electrode [adjoining a couple by carrying out]. The process which forms an orientation film on the portion of the aforementioned insulator layer between the 3rd layer with which the aforementioned pixel electrode top and the aforementioned pixel electrode are not formed. The process which carries out rubbing processing of this orientation film in the direction which met the aforementioned capacity line side from the aforementioned scanning-line side to the scanning line and the capacity line of the aforementioned couple at the other aforementioned data line.

[Claim 18] The manufacture method of the liquid crystal equipment characterized by providing the following. The process which is the manufacture method of liquid crystal equipment according to claim 13, and forms the aforementioned shading film in the predetermined field on aforementioned one substrate. The process which forms the aforementioned insulator layer between the 1st layer on aforementioned one substrate and a shading film so that the portion corresponding to the aforementioned position by which connection is made may become depressed in the aforementioned concave. The process which forms the aforementioned TFT on the aforementioned insulator layer between the 1st layer. The process which forms an insulator layer between the 2nd layer on an insulator layer between the aforementioned TFT and the 1st layer, As a contact hole for connecting the wiring from the aforementioned constant source of potential as the aforementioned shading film As a contact hole for connecting the aforementioned TFT and the aforementioned data line between the above 2nd and the 1st layer at the same time it punctures an insulator layer until it results in the aforementioned shading film in the aforementioned position by which connection is made The process which punctures an insulator layer between the above 2nd and the 1st layer until it results in the aforementioned semiconductor layer in the position which counters the source or the drain field of a semiconductor layer which constitutes the aforementioned TFT.

[Claim 19] Electronic equipment characterized by equipping claims 1-13 with the liquid crystal equipment of a publication.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[The technical field to which invention belongs] this invention belongs to the technical field of the liquid crystal equipment of the active-matrix drive method by TFT (TFT is called hereafter) drive, its manufacture method, and the electronic equipment using this.

[0002]

[Description of the Prior Art] Conventionally, in this kind of liquid crystal equipment, the orientation film of a couple with which rubbing processing was performed in the predetermined direction is respectively prepared on the pixel electrode and the counterelectrode between the substrates of a couple, and liquid crystal is pinched in the state of predetermined orientation among these orientation films. And at the time of operation, electric field are impressed to this liquid crystal from two electrodes, the orientation state of liquid crystal

changes and a display is performed in the screen-display field of liquid crystal equipment.

[0003] Therefore, the field which formed wiring of the data line, the scanning line, a capacity line, etc. in this kind of liquid crystal equipment, Supposing it leaves the irregularity by the difference of the sum total thickness on a TFT array substrate with the fields (opening field through which the incident light for image display passes especially) in which these data lines etc. are not formed even to the field (orientation film) which touches liquid crystal as it is temporarily According to the grade of the irregularity, poor orientation (disclination) occurs in liquid crystal, and it leads to degradation of the picture of each pixel. In having performed rubbing processing to the orientation film more specifically formed on the concavo-convex side where each opening field became depressed, according to this irregularity, dispersion in orientation restraining force arises on an orientation film front face, it is this concavo-convex section, and the poor orientation of liquid crystal will occur and contrast will change. That is, while a white omission phenomenon will happen in the part where orientation is poor and contrast will fall if the poor orientation of liquid crystal happens, and it is the normally white mode which serves as a white display at the time of liquid crystal voltage un-impressing for example, a definition will also fall. In the distance between orientation films (thickness of liquid crystal), in order to maintain at a predetermined value, to go across the rubbing processing to an orientation film all over a substrate and to give equally and appropriately, it is important equal and to carry out flattening of the pixel section located in a screen-display field to avoid such a situation.

[0004] On the other hand, in this kind of liquid crystal equipment, even if the duty ratio at the time of supplying a picture signal to each pixel electrode is small, in order to make it neither a flicker nor a cross talk occur, the storage capacitance which gives predetermined capacity to each pixel electrode is prepared.

[0005] Here, in this kind of liquid crystal equipment, in order for the request of gathering a pixel numerical aperture and making a screen bright to also make such a storage capacitance increase for a certain reason, the storage capacitance like **** is formed in the field in alignment with the bottom of the data line which consists of un-transparence aluminum (aluminum) in the position corresponding to the shading layer prepared in an opposite substrate as a boundary of a contiguity pixel etc., or the data line. The semiconductor layer more specifically installed in the bottom of the data line from the semiconductor layer which constitutes TFT in the pixel section when it was a field under the data line is

formed as the 1st storage-capacitance electrode. The capacity line which forms the insulator layer which consists of the same film as a gate insulator layer on this 1st storage-capacitance electrode, consists of contest low resistance polysilicon of the still more nearly same layer as the scanning line etc., and is arranged along with the scanning line is installed on the insulator layer. It forms as the 1st storage-capacitance electrode and the 2nd storage-capacitance electrode which counters through an insulator layer. Or if it is a field in alignment with the scanning line, while forming the semiconductor layer installed in the bottom of a capacity line from the semiconductor layer which constitutes TFT in the pixel section as the 1st storage-capacitance electrode, the insulator layer which consists of the same film as a gate insulator layer is formed on this 1st storage-capacitance electrode (the 1st storage-capacitance electrode and the portion of the capacity line which counters through an insulator layer function as the 2nd storage-capacitance electrodes in this case).

[0006] High definition image display is made possible by fully taking such a storage capacitance.

[0007]

[Problem(s) to be Solved by the Invention] However, if a storage capacitance is made as mentioned above to the field under the data line, or the field in alignment with the scanning line, the thickness of this portion will increase and a comparatively big level difference will be made to the pixel section. For example, if a storage capacitance is made to the field under the data line, only the thickness (the 1st storage-capacitance electrode, an insulator layer, and thickness of the sum total of 2 storage-capacitance electrode) of a storage capacitance and the thickness of the data line will become a bird clapper from the pixel section in which these do not exist highly, and the level difference will also become about 10000 NA. If there is such a level difference, rubbing processing will no longer be appropriately performed in the level difference portion concerned. Consequently, the poor orientation of the above liquid crystal happens along with the data line, and the trouble that contrast and a definition fall arises.

[0008] On the contrary, if flattening of the front face whose level difference increased by having made the storage capacitance in this way is carried out as mentioned above, manufacture efficiency and cost will get worse. if it is going to perform flattening of the pixel section after forming a storage capacitance in the field under the data line as mentioned above especially -- the [the 1st and] -- since the sum total thickness of a data-line portion which piled up even the layer insulation film which is needed

along with 2 storage-capacitance electrode, the insulator layer for capacity formation, or this wiring increases, the burden to a flattening process increases and there is a trouble that manufacture efficiency and cost will get worse very much

[0009] this invention is made in view of the trouble mentioned above, and the poor orientation of liquid crystal to which a storage capacitance leads to quality-of-image degradation greatly makes it a technical problem to offer electronic equipment equipped with the liquid crystal equipment reduced as much as possible, its manufacture method, and the liquid crystal equipment concerned.

[0010]

[Means for Solving the Problem] In order that liquid crystal equipment according to claim 1 may solve the above-mentioned technical problem, it comes to enclose liquid crystal between the substrates of a couple. The data line of plurality [top / substrate / of the substrate of this couple / one], Two or more scanning lines which intersect two or more of these data lines, and two or more TFT respectively connected to the data line and the scanning line of the aforementioned plurality, Two or more pixel electrodes which were respectively connected to two or more of these TFT, and have been arranged more nearly up than the aforementioned data line, Two or more 1st storage-capacitance polar zone which consisted of the same material as the semiconductor layer which constitutes the drain or source field of two or more of these TFT, and was respectively installed in the bottom of the aforementioned data line at least, Two or more capacity lines which contain respectively the 2nd storage-capacitance polar zone by which opposite arrangement was respectively carried out through the 1st storage-capacitance polar zone and insulator layer of the aforementioned plurality under the aforementioned data line, It has at least one layer insulation film arranged between aforementioned one substrate and the aforementioned pixel electrode, and the field which counters the aforementioned 2nd storage-capacitance polar zone which is under the aforementioned data line at least among the aforementioned capacity lines is become depressed and formed in a concave, and the aforementioned layer insulation film is characterized by the bird clapper.

[0011] According to liquid crystal equipment according to claim 1, the 1st storage-capacitance polar zone consists of the same material as the semiconductor layer which constitutes the drain or source field of TFT, and is respectively installed in the bottom of the data line at least. Opposite arrangement of the 2nd storage-capacitance polar zone is respectively carried out through the 1st

storage-capacitance polar zone and the insulator layer under the data line at least. Thus, according to this invention, since an incident light does not penetrate, the space under the data line unusable as an opening field is effectively used as a space for giving capacity to a pixel electrode.

[0012] Moreover, according to this invention, the field which counters the 2nd storage-capacitance polar zone which is under the data line at least among capacity lines becomes depressed in a concave compared with other fields, and the layer insulation film is formed. Therefore, flattening of the pixel electrode side located above the data line is carried out by this hollow. For example, if only the depth equal to the 1st storage-capacitance polar zone, an insulator layer, the 2nd storage-capacitance polar zone, and the sum total thickness of the data line is hollowed to a concave, flattening of the pixel electrode side will be carried out nearly completely.

[0013] As mentioned above, although it originates in the ability of rubbing processing to have not been appropriately performed with a level difference conventionally, or it originates in the deviation of the distance between substrates by the level difference directly and the poor orientation of liquid crystal tended to occur in the portion in alignment with the data line of this opening field, according to this invention, the poor orientation in this portion can be reduced by flattening.

[0014] In order that liquid crystal equipment according to claim 2 may solve the above-mentioned technical problem, it comes to enclose liquid crystal between the substrates of a couple. The data line of plurality [top / substrate / of the substrate of this couple / one], Two or more scanning lines which intersect two or more of these data lines, and two or more TFT respectively connected to the data line and the scanning line of the aforementioned plurality, Two or more 1st storage-capacitance polar zone which consisted of the same material as two or more pixel electrodes respectively connected to two or more of these TFT, and the semiconductor layer which constitutes the drain or source field of two or more of these TFT, and was respectively installed in the bottom of the aforementioned data line at least, Two or more capacity lines which contain respectively the 2nd storage-capacitance polar zone by which opposite arrangement was respectively carried out through the 1st storage-capacitance polar zone and insulator layer of the aforementioned plurality under the aforementioned data line, The insulator layer between the 1st layer arranged between aforementioned one substrate and the aforementioned 1st storage-capacitance polar zone, The

insulator layer between the 2nd layer arranged between the aforementioned 2nd storage-capacitance polar zone and the aforementioned data line, It has the insulator layer between the 3rd layer arranged between the aforementioned data line and the aforementioned pixel electrode. among insulator layers between the above 1st, the 2nd, and the 3rd layer at least one insulator layer It is characterized by becoming depressed and forming in a concave the field which counters the aforementioned 2nd storage-capacitance polar zone which is under the aforementioned data line at least among the aforementioned capacity lines.

[0015] According to liquid crystal equipment according to claim 2, the 1st storage-capacitance polar zone consists of the same material as the semiconductor layer which constitutes the drain or source field of TFT, and is respectively installed in the bottom of the data line at least. Opposite arrangement of the 2nd storage-capacitance polar zone is respectively carried out through the 1st storage-capacitance polar zone and the insulator layer under the data line at least. Thus, according to this invention, since an incident light does not penetrate, the space under the data line unusable as an opening field is effectively used as a space for giving capacity to a pixel electrode.

[0016] on the other hand, the insulator layer between the 1st layer -- the [one substrate and] -- it is arranged between 1 storage-capacitance polar zone, the insulator layer is arranged between the 2nd storage-capacitance polar zone and the aforementioned data line between the 2nd layer, and the insulator layer is arranged between the data line and the pixel electrode between the 3rd layer.A level difference can do only the part to which the laminating of the data line which the field where the data line is generally wired becomes from the 2nd storage-capacitance polar zone of the capacity line which consists of the same polysilicon contest layer as the 1st storage-capacitance polar zone which consists of the same material as a semiconductor layer as compared with the pixel section located in an opening field, an insulator layer, and the scanning line etc., aluminum film, etc. is carried out here. And this level difference is largest level difference as compared with the pixel section located on the structure of liquid crystal equipment, and in an opening field. However, between the 1st, the 2nd, and the 3rd layer, among insulator layers, the field which counters the 2nd storage-capacitance polar zone which is under the data line at least among capacity lines becomes depressed in a concave compared with other fields, and, according to this invention, at least one insulator layer is formed. Therefore, according to this hollow, flattening of the

pixel electrode side formed the upper surface of an insulator layer or on this is carried out between the 3rd layer located above the data line. For example, if only the depth equal to the 1st storage-capacitance polar zone, the insulator layer for capacity formation, the 2nd storage-capacitance polar zone, and the sum total thickness of the data line is hollowed to a concave, flattening of the pixel electrode side formed the upper surface of an insulator layer or on this between the 3rd layer will be carried out nearly completely.

[0017] As mentioned above, although it originates in the ability of rubbing processing to have not been appropriately performed with a level difference conventionally, or it originates in the deviation of the distance between substrates by the level difference directly and the poor orientation of liquid crystal tended to occur in the portion in alignment with the data line of this opening field, according to this invention, the poor orientation in this portion can be reduced by flattening.

[0018] Liquid crystal equipment according to claim 3 is set to liquid crystal equipment according to claim 2, in order to solve the above-mentioned technical problem. Two or more aforementioned 1st storage-capacitance polar zone is respectively installed in the scanning line of further the aforementioned plurality, and parallel. Opposite arrangement of two or more aforementioned 2nd storage-capacitance polar zone is further carried out through the aforementioned scanning line, the aforementioned 1st storage-capacitance polar zone installed in parallel, and the aforementioned insulator layer for capacity formation. the above -- it is characterized by becoming depressed and forming in a concave the field where one insulator layer counters the aforementioned 2nd storage-capacitance polar zone parallel to the aforementioned scanning line among the aforementioned capacity lines further even if few

[0019] According to liquid crystal equipment according to claim 3, in the field where the 1st storage-capacitance polar zone and the 2nd storage-capacitance polar zone are parallel to the scanning line, opposite arrangement is carried out through the insulator layer for capacity formation. Thus, according to this invention, it is effectively used as a space for not only the bottom of the data line but a field parallel to the scanning line giving capacity to a pixel electrode. if the field where a capacity line is wired in parallel with the scanning line is generally compared with the pixel section located in an opening field here -- the [the 1st storage-capacitance polar zone, the insulator layer for capacity formation, and] -- a level difference can do only the part to which the laminating of the 2

storage-capacitance polar zone is carried out However, between the 1st, the 2nd, and the 3rd layer, among insulator layers, the field which counters the 2nd storage-capacitance polar zone parallel to the scanning line at least among capacity lines becomes depressed in a concave, and, according to this invention, at least one insulator layer is formed. Therefore, according to this hollow, flattening of the pixel electrode side formed the upper surface of an insulator layer or on this is carried out between the 3rd layer located above this capacity line. the [for example, / the 1st storage-capacitance polar zone the insulator layer for capacity formation, and] -- if only the depth equal to the sum total thickness of 2 storage-capacitance polar zone is hollowed to a concave, flattening of the pixel electrode side formed the upper surface of an insulator layer or on this between the 3rd layer will be carried out nearly completely

[0020] Liquid crystal equipment according to claim 4 is set to liquid crystal equipment according to claim 3, in order to solve the above-mentioned technical problem. The orientation film by which rubbing processing was carried out in the direction which met the aforementioned capacity line side from the aforementioned scanning-line side at the other aforementioned data line to the scanning line and the capacity line of a couple which are arranged on the aforementioned pixel electrode and put in order adjacently, It is characterized by having packed the scanning line and the capacity line of the aforementioned couple in the one band section in alignment with the aforementioned scanning line, and having a wrap shading layer further.

[0021] According to liquid crystal equipment according to claim 4, in the TFT array substrate, the orientation film is arranged on the pixel electrode and rubbing processing is carried out in the direction which met the capacity line side from the scanning-line side to the scanning line and the capacity line of a couple which were put in order adjacently at the other data line. Generally, to the level difference to which a field becomes high in the direction of rubbing, rubbing processing was performed comparatively good, and it has become clear that it is difficult to perform rubbing processing good to the level difference to which a field becomes low in the direction of rubbing here as a result of research by this invention person. Then, if it is made to perform rubbing processing in the direction towards the capacity line side which gave flattening like this invention from the scanning-line side which has not given flattening, since the level difference in one edge of the scanning line by the side of the pixel located in the upstream of the direction of rubbing turns into a level difference to which a field becomes high in the direction of rubbing, rubbing

processing will be performed good. On the other hand, since the level difference in the edge of another side of the scanning line of the side which adjoins a capacity line turns into a level difference to which a field becomes low in the direction of rubbing, rubbing processing is not performed good. However, since it is collectively covered by the one band section of a shading layer while the field which is located above a capacity line and by which flattening was carried out is between this portion and the pixel located in the lower stream of a river of the direction of rubbing, it is distantly [from an opening field] separated. for this reason, the thing for which the poor orientation of the liquid crystal by this influences a picture even if rubbing processing is not performed good corresponding to the edge of another side of the scanning line -- most -- or there is completely nothing Temporarily, if the direction of rubbing processing is carried out reversely, you have to narrow an opening field by the level difference to which a field becomes low in the direction of rubbing appearing in the edge of the scanning line of the one distant from a capacity line, and the poor orientation of the liquid crystal by this affecting a picture, or covering such a portion in a shading layer further.

[0022] Furthermore, when the direction of rubbing of a TFT array substrate is made to meet the data line, Although the scanning-line reversal drive method (1H reversal drive method) which reverses the voltage polarity which drives liquid crystal for every scanning line is becoming common in order not to degrade liquid crystal by direct-current drive, and in order to prevent the flicker of a display image According to this scanning-line reversal drive method, it has become clear that the poor orientation (disclination) of liquid crystal tends to occur with the level difference of the pixel section in near the scanning line which is a level difference of the direction of the data line as a result of research by this invention person. Then, when the level difference of the direction of the data line constituted like this invention so that it might come not between the edge of the scanning line of a couple, and a capacity line but between the scanning lines of this couple and capacity lines and an above-mentioned scanning-line reversal drive method is adopted, it can occur in the field distant from each pixel opening field so that the poor orientation of liquid crystal may occur near the center of a pixel border area. Consequently, this invention is very advantageous, when attaining raise in contrast, and highly minute-ization, in case a scanning-line reversal drive method is used.

[0023] liquid crystal equipment given in either of the claims 2-4 in order that liquid crystal equipment according to claim 5 may solve the above-mentioned

technical problem -- setting -- the above -- it is characterized by one insulator layer consisting of monolayers, even if few

[0024] Since what is necessary is just to constitute the insulator layer formed in a concave by becoming depressed from a monolayer according to liquid crystal equipment according to claim 5, even if it compares with the conventional case, there is no need of making the number of layers increasing, and if the thickness of the portion which became depressed in the concave, and the portion which is not so is controlled, the insulator layer formed in the concave concerned by becoming depressed will be obtained.

[0025] liquid-crystal equipment given in claims 2-4 in order that liquid-crystal equipment according to claim 6 may solve the above-mentioned technical problem -- setting -- the above -- it is characterized by for one insulator layer to consist of a monolayer portion and a multilayer portion, even if few, and to consider as the portion to which the aforementioned monolayer portion became depressed in the aforementioned concave, and to consider as the portion to which the aforementioned multilayer portion has not become depressed in the aforementioned concave

[0026] Since the monolayer portion is used as the portion which became depressed in the concave according to liquid crystal equipment according to claim 6, thickness of the insulator layer in which the hollow concerned in the portion which became depressed in the concave was formed is made comparatively easy as thickness of a monolayer portion, and can be controlled certainly and with high precision. Therefore, it also becomes possible to make very thin thickness of the insulator layer in which the hollow concerned in the portion which became depressed in this concave was formed.

[0027] In order that liquid crystal equipment according to claim 7 may solve the above-mentioned technical problem, in liquid crystal equipment given in any 1 term of claims 2-6, an insulator layer is characterized by consisting of a silicon-oxide film or a silicon nitride film between the above 1st and the 2nd layer.

[0028] According to liquid crystal equipment according to claim 7, between the 1st which consists of a silicon-oxide film or a silicon nitride film, and the 2nd layer, while being able to carry out the electric insulation of each class which constitutes one substrate, the 1st storage-capacitance electrode section, the 2nd storage-capacitance electrode section, the data line, etc. mutually, the contamination to TFT from one substrate etc. can be prevented by the insulator layer. And the insulator layer is suitable for the ground film of TFT between the 1st layer constituted in this way.

[0029] In liquid crystal equipment given in any 1 term of claims 2-7 in order that

liquid crystal equipment according to claim 8 may solve the above-mentioned technical problem Aforementioned one substrate serves as the aforementioned insulator layer between the 1st layer, and at least one side is characterized by becoming depressed and forming in a concave the field which counters the aforementioned 2nd storage-capacitance electrode section which is under the aforementioned data line at least among the aforementioned capacity lines among insulator layers between the above 2nd and the 3rd layer.

[0030] According to liquid crystal equipment according to claim 8, one substrate serves as the insulator layer between the 1st layer. That is, one substrate functions also as a ground film of TFT, and an insulator layer is omitted between the 1st layer. However, according to this invention, between the 2nd and the 3rd layer, among insulator layers, since the field which counters the 2nd storage-capacitance electrode section which at least one side has under the data line at least among capacity lines becomes depressed in a concave and it is formed, flattening of the upper surface of an insulator layer or a pixel electrode side is attained between the 3rd layer like an above-mentioned this invention.

[0031] It is characterized by having further the shading film prepared in the position of two or more aforementioned TFT with which the field for channel formation is seen from aforementioned one substrate side at least, and it laps respectively between the aforementioned substrate and the aforementioned insulator layer between the 1st layer in liquid crystal equipment given in any 1 term of claims 2-7, in order that liquid crystal equipment according to claim 9 may solve the above-mentioned technical problem.

[0032] According to liquid crystal equipment according to claim 9, the shading film is prepared in one substrate in the position of two or more TFT with which the field for channel formation is seen from one substrate side at least, and it laps respectively. Therefore, the situation in which the return light from one substrate side etc. carries out incidence to the field for channel formation concerned can be prevented, and the property of TFT does not deteriorate by generating of a photocurrent. And the shading film is prepared between one substrate and the insulator layer between the 1st layer. Therefore, while being able to carry out the electric insulation of the TFT etc. from a shading film, the situation where a shading film pollutes TFT etc. can be prevented.

[0033] Liquid crystal equipment according to claim 10 is set to liquid crystal equipment according to claim 9, in order to solve the above-mentioned technical problem. the aforementioned

shading film The 3rd storage-capacitance electrode section prepared in at least one side and the position which counters through the aforementioned insulator layer between the 1st layer is included among the portion under the aforementioned data line of the aforementioned 1st storage-capacitance electrode section, and the portion parallel to the aforementioned scanning line. The aforementioned insulator layer between the 1st layer is characterized by becoming depressed and forming the field between the aforementioned 3rd storage-capacitance electrode section and the aforementioned 1st storage-capacitance electrode section in the aforementioned concave.

[0034] According to liquid crystal equipment according to claim 10, the shading film contains at least one side and the 3rd storage-capacitance electrode section prepared in the position which counters through an insulator layer between the 1st layer among the portion under the data line of the 1st storage-capacitance electrode section, and the portion parallel to the scanning line. Therefore, in addition to the capacity formed in the 1st storage-capacitance electrode section by which opposite arrangement was carried out through the insulator layer for capacity formation, and the 2nd storage-capacitance electrode section, the capacity formed in the 1st storage-capacitance electrode section by which opposite arrangement was carried out through the insulator layer between the 1st layer, and the 3rd storage-capacitance electrode section is also given to a pixel electrode as a storage capacitance. Generally the capacity formed, so that the capacity formed, so that the thickness of the insulator layer by which it is placed in between between capacity formation is thick is small and it is thin becomes large here. However, according to this invention, between the 1st layer, since the field between the 3rd storage-capacitance electrode section and the 1st storage-capacitance electrode section is become depressed and formed in the concave, an insulator layer can make thin thickness of the insulator layer by which it is placed in between between capacity formation according to the depth of a concave hollow. the [consequently, / the 1st and] -- capacity can be increased efficiently, without increasing the surface area of 3 storage-capacitance electrode section

[0035] In order that liquid crystal equipment according to claim 11 may solve the above-mentioned technical problem, in liquid crystal equipment according to claim 9 or 10, the aforementioned shading film is characterized by including at least one of Ti (titanium), Cr (chromium), W (tungsten), Ta (tantalum), Mo (molybdenum), and Pd (lead).

[0036] A shading film contains at least one of Ti, Cr, W, Ta, Mo, and Pd which are an opaque refractory metal, for example, since it consists of a metal simple substance, an alloy, metal silicide, etc., a shading film is destroyed by high temperature processing in the TFT formation process performed after the shading film formation process on a TFT array substrate, or it can be prevented from fusing it by it according to liquid crystal equipment according to claim 11.

[0037] In order that liquid crystal equipment according to claim 12 may solve the above-mentioned technical problem, in liquid crystal equipment given in any 1 term of claims 9-11, the aforementioned shading film is characterized by connecting with the constant source of potential.

[0038] According to liquid crystal equipment according to claim 12, since the shading film is connected to the constant source of potential, let a shading film be constant potential. Therefore, potential change of a shading film does not have a bad influence on a shading film to TFT by which opposite arrangement is carried out.

[0039] In order that liquid crystal equipment according to claim 13 may solve the above-mentioned technical problem, in liquid crystal equipment according to claim 12, the aforementioned insulator layer between the 1st layer is characterized by being punctured while being become depressed and formed in the aforementioned concave in the position where the aforementioned constant source of potential is connected as the aforementioned shading film.

[0040] According to liquid crystal equipment according to claim 13, between the 1st layer, since it is become depressed and formed in the concave in the position where a shading film and the constant source of potential are connected, an insulator layer becomes easy [the process which punctures this position] in the manufacture process according to the depth of the portion which became depressed in this concave after insulator layer formation between the 1st layer concerned.

[0041] The process which deposits the insulator layer which is the manufacture method of liquid crystal equipment according to claim 5 in order that the manufacture method of liquid crystal equipment according to claim 14 may solve the above-mentioned technical problem, and should constitute the aforementioned monolayer, It is characterized by having the process which forms the resist pattern corresponding to the portion which became depressed in the deposited this insulator layer at the aforementioned concave by the photolithography, and the etching process which forms the portion which etched the predetermined time through this resist pattern, and became

depressed in the aforementioned concave.

[0042] According to the manufacture method of liquid crystal equipment according to claim 14, the insulator layer which should constitute the aforementioned monolayer from on one substrate accumulates throughout a screen-display field first. Next, the resist pattern corresponding to the portion which became depressed in the deposited this insulator layer at the concave is formed by the photolithography, after that, etching is performed only for a predetermined time through this resist pattern, and the portion which became depressed in the concave is formed. Therefore, the depth and thickness of a portion which became depressed in the concave are controllable by the time management of etching. In this etching process, when using dry etching, it can puncture mostly as an exposure size.

[0043] The process which deposits the 1st insulator layer which is the manufacture method of liquid crystal equipment according to claim 6 in order that the manufacture method of liquid crystal equipment according to claim 15 may solve the above-mentioned technical problem, and should constitute the aforementioned multilayer portion, The process which forms the resist pattern corresponding to the portion which became depressed in the 1st deposited this insulator layer at the aforementioned concave by the photolithography, The etching process which removes the 1st insulator layer of the above corresponding to the portion which etched through this resist pattern and became depressed in the aforementioned concave, It is characterized by having the process which deposits the 2nd insulator layer which should constitute the aforementioned monolayer portion and a multilayer portion on the field which removed the 1st insulator layer of the above, and the 1st insulator layer of the above.

[0044] According to the manufacture method of liquid crystal equipment according to claim 15, the 1st insulator layer which should constitute a multilayer portion from on one substrate accumulates throughout a screen-display field first. Next, the resist pattern corresponding to the portion which became depressed in the concave is formed in this 1st deposited insulator layer by the photolithography, etching is performed through this resist pattern after that, and the 1st insulator layer corresponding to the portion which became depressed in the concave is removed. Then, the 2nd insulator layer which should constitute a monolayer portion and a multilayer portion accumulates on the field which removed the 1st insulator layer and the 1st insulator layer. Consequently, thickness of the insulator layer between the 1st

layer in the portion which became depressed in the concave is made comparatively easy, and can be controlled by management of the thickness of the 2nd insulator layer certainly and with high precision. In this etching process, when using dry etching, it can puncture mostly as an exposure size.

[0045] In order that the manufacture method of liquid crystal equipment according to claim 16 may solve the above-mentioned technical problem, it is the manufacture method of liquid crystal equipment according to claim 14 or 15, and the aforementioned etching process is characterized by including the wet etching process which forms the side attachment wall of the portion which became depressed in the aforementioned concave at least in the shape of a taper.

[0046] According to the manufacture method of liquid crystal equipment according to claim 16, the side attachment wall of the portion which became depressed in the concave is formed in the shape of a taper of a wet etching process. Thus, if the side attachment wall of the portion which became depressed in the concave is formed in the shape of a taper, in the portion which became depressed in the concave, at a back process, it will be formed, for example, a polysilicon contest film etc. will not remain. For this reason, flattening of this portion can be carried out certainly. Moreover, it cannot be overemphasized that dry etching and wet etching may be combined.

[0047] In order that the manufacture method of liquid crystal equipment according to claim 17 may solve the above-mentioned technical problem, it is the manufacture method of liquid crystal equipment given in any 1 term of claim 14 and others [16]. The process formed on the aforementioned insulator layer between the 1st layer so that the aforementioned scanning line and a capacity line may be arranged in the aforementioned pixel inter-electrode [adjoining a couple by carrying out], The process which forms an orientation film on the portion of the aforementioned insulator layer between the 3rd layer with which the aforementioned pixel electrode top and the aforementioned pixel electrode are not formed, It is characterized by having the process which carries out rubbing processing of this orientation film in the direction which met the aforementioned capacity line side from the aforementioned scanning-line side to the scanning line and the capacity line of the aforementioned couple at the other aforementioned data line.

[0048] According to the manufacture method of liquid crystal equipment according to claim 17, the scanning line and a capacity line are formed on an insulator layer between the 1st layer so that the scanning line and the capacity

line of a couple may be located in a line with the pixel inter-electrode which adjoins each other. Next, while [the 3rd layer] the pixel electrode top and the pixel electrode are not formed, an orientation film is formed on the portion of an insulator layer. And next, rubbing processing of this orientation film is carried out in the direction which met the capacity line side from the scanning-line side to the scanning line and the capacity line of a couple at the other data line. therefore, the thing for which the poor orientation of the liquid crystal in near [this] an edge influences a picture since the edge where rubbing processing of the scanning line located in the upstream of the direction of rubbing is not performed good as mentioned above is distant from the opening field -- most -- or there is completely nothing It is very advantageous, when attaining raise in contrast, and highly minute-ization, in case a scanning-line reversal drive method is used especially as mentioned above.

[0049] The process which is the manufacture method of liquid crystal equipment according to claim 13 in order that the manufacture method of liquid crystal equipment according to claim 18 may solve the above-mentioned technical problem, and forms the aforementioned shading film in the predetermined field on aforementioned one substrate, The process which forms the aforementioned insulator layer between the 1st layer on aforementioned one substrate and a shading film so that the portion corresponding to the aforementioned position by which connection is made may become depressed in the aforementioned concave, The process which forms Above TFT on the aforementioned insulator layer between the 1st layer, and the process which forms an insulator layer between the 2nd layer on an insulator layer between Above TFT and the 1st layer, As a contact hole for connecting the wiring from the aforementioned constant source of potential as the aforementioned shading film As a contact hole for connecting Above TFT and the aforementioned data line between the above 2nd and the 1st layer at the same time it punctures an insulator layer until it results in the aforementioned shading film in the aforementioned position by which connection is made It is characterized by having the process which punctures the aforementioned insulator layer between the 2nd layer until it results in the aforementioned semiconductor layer in the position which counters the source or the drain field of a semiconductor layer which constitutes Above TFT.

[0050] According to the manufacture method of liquid crystal equipment according to claim 18, an insulator layer is formed between the 1st layer on a substrate and this shading film so that

the portion corresponding to the position where a shading film is formed in the predetermined field on one substrate, and a shading film and the constant source of potential are connected may become depressed in a concave in while. Then, TFT is formed on an insulator layer between the 1st layer, and an insulator layer is further formed between the 2nd layer on an insulator layer between TFT and the 1st layer. Between this 2nd layer, an insulator layer is prepared in electric insulation, such as TFT, the data line, the scanning line, and a capacity line. Here, as a contact hole for connecting a shading film and the wiring from the constant source of potential, the 2nd and the insulator layer between the 1st layer are punctured, and as a contact hole for connecting TFT and the data line simultaneously until it results in a shading film, an insulator layer is punctured between the 2nd layer until it results in a semiconductor layer. Therefore, these two kinds of contact holes can be punctured collectively.

[0051] It is characterized by electronic equipment according to claim 19 equipping claims 1-13 with the liquid crystal equipment of a publication, in order to solve the above-mentioned technical problem.

[0052] According to electronic equipment according to claim 19, electronic equipment is equipped with the liquid crystal equipment of the invention in this application mentioned above, and the high-definition image display of it becomes possible with few liquid crystal equipment with the faulty orientation of liquid crystal by the pixel electrode by which flattening was carried out.

[0053] Such an operation and other gains of this invention are made clear from the gestalt of the operation explained below.

[0054]

[Embodiments of the Invention] Hereafter, the gestalt of operation of this invention is explained based on a drawing.

[0055] (Gestalt of operation of the 1st of liquid crystal equipment) The composition and operation of the gestalt of operation of the 1st of liquid crystal equipment by this invention are explained based on drawing 8 from drawing 1 . Drawing 1 is the plan of the pixel section in the opening field of a TFT array substrate in which the data line, the scanning line, the pixel electrode, the shading film, etc. were formed. Drawing 2 is the plan for a connection of a shading film and a constant potential line. Drawing 3 is the cross section of the liquid crystal equipment in which the A-A' cross section of drawing 1 is shown with an opposite substrate etc. Drawing 4 is the B-B' cross section of drawing 1, and drawing 5 is the C-C' cross section of drawing 1. Moreover, drawing 6 is the D-D' cross section of drawing 2 . In addition, in order to make each class and

each part material into the size of the grade which can be recognized on a drawing in drawing 6 from drawing 3 , scales are made to have differed for each class or every each part material.

[0056] In drawing 1, on the TFT array substrate of liquid crystal equipment, two or more transparent pixel electrode 9a (the profile is shown by dotted-line section 9a') is prepared in the shape of a matrix, and data-line 6a (source electrode), scanning-line 3a (gate electrode), and capacity line 3b are prepared respectively along the boundary of pixel electrode 9a in every direction. Electrical installation of the data-line 6a is carried out to the below-mentioned source field among semiconductor layer 1a which consists of a polysilicon contest film through contact hole 5a, and electrical installation of the pixel electrode 9a is carried out to the below-mentioned drain field among semiconductor layer 1a through the contact hole 8. Moreover, scanning-line 3a (gate electrode) is arranged so that below-mentioned field 1a' for channel formation (field of the slash of drawing Nakamigi going down) may be countered among semiconductor layer 1a. And shading film 11a in the pixel section is prepared in the field shown with the slash of the upward slant to the right in drawing. That is, shading film 11a is prepared in the position with which TFT containing field 1a' for channel formation of semiconductor layer 1a, data-line 6a, scanning-line 3a, and capacity line 3b are seen from a TFT array substrate side, and it laps respectively in the pixel section.

[0057] In the field surrounded by the thick line containing capacity line 3b formed in the bottom of data-line 6a especially in drawing 1 , the below-mentioned insulator layer between the 1st layer is become depressed and formed in the concave, and the insulator layer is mostly formed relatively between the 1st layer concerned convex in the field corresponding to the other pixel electrode 9a and scanning-line 3a (to plane). Moreover, if it is made to perform the direction of rubbing of the TFT array substrate 10 in the direction of the arrow of drawing 1 , especially the gestalt of this operation will demonstrate an effect.

[0058] Therefore, the poor orientation [according to / although it was easiest to occur in the portion to which it originated in the deviation of the distance between the substrates originate in the ability of rubbing processing to have not been appropriately performed with the level difference in which the data line is formed conventionally, and to which the forming face of an orientation film becomes high most, or according to such a level difference directly, and the poor orientation of liquid crystal met the data line of this opening field / the gestalt of this operation] in this portion can be

reduced by

[0059] In drawing 2 , constant potential line 6b formed from conductive layers, such as the same aluminum as data-line 6a, is prepared on the TFT array substrate of liquid crystal equipment, and it connects with shading film (shading wiring) 11b in the non-pixel section through contact hole 5b. In field 5C surrounded by the thick line which contains contact hole 5b especially in drawing 2 , the below-mentioned insulator layer between the 1st layer is become depressed and formed in the concave, and the insulator layer is relatively formed between the 1st layer concerned in the other field convex (to plane).

[0060] As shown in drawing 6 from drawing 3 , while is transparent and liquid crystal equipment 100 is equipped with the TFT array substrate 10 which constitutes an example of a substrate, and the opposite substrate 20 by which opposite arrangement is carried out at this and which it is transparent and also constitutes an example of the substrate of a way. The TFT array substrate 10 consists for example, of a quartz substrate, and the opposite substrate 20 consists of a glass substrate or a quartz substrate. Pixel electrode 9a is prepared in the TFT array substrate 10, and the orientation film 19 with which predetermined orientation processing of rubbing processing etc. was performed is formed in the bottom. Pixel electrode 9a consists of transparent conductivity thin films, such as for example, an ITO film (indium teens oxide film). Moreover, the orientation film 19 consists of organic thin films, such as for example, a polyimide thin film.

[0061] On the other hand, it crosses to the opposite substrate 20 all over the, the counterelectrode (common electrode) 21 is formed, and the orientation film 22 with which predetermined orientation processing of rubbing processing etc. was performed is formed in the bottom. A counterelectrode 21 consists of transparent conductivity thin films, such as for example, an ITO film. Moreover, the orientation film 22 consists of organic thin films, such as a polyimide thin film.

[0062] As shown in drawing 3 , TFT30 for pixel switching which carries out switching control of each pixel electrode 9a is formed in the position which adjoins each pixel electrode 9a at the TFT array substrate 10.

[0063] As further shown in the opposite substrate 20 at drawing 3 , the shading layer 23 is formed in fields other than the opening field of each pixel. For this reason, an incident light trespasses neither upon field 1a' for channel formation of semiconductor layer 1a of TFT30 for pixel switching, nor the LDD (Lightly Doped Drain) fields 1b and 1c from the opposite substrate 20 side. Furthermore, the shading layer 23 has

functions, such as improvement in contrast, and color mixture prevention of color material.

[0064] Thus, it is constituted, and between the TFT array substrates 10 and the opposite substrates 20 which have been arranged so that pixel electrode 9a and a counterelectrode 21 may meet, liquid crystal is enclosed with the space surrounded by the below-mentioned sealant 52 (refer to drawing 13 and drawing 14), and the liquid crystal layer 50 is formed. The liquid crystal layer 50 takes a predetermined orientation state with the orientation films 19 and 22 in the state where the electric field from pixel electrode 9a are not impressed. The liquid crystal layer 50 consists of liquid crystal which mixed the pneumatic liquid crystal of a kind or some kinds. It is the adhesives which consist of a photoresist or thermosetting resin in order that a sealant 52 may stick two substrates 10 and 20 around those, and spacers, such as glass fiber for making distance between both substrates into a predetermined value or a glass bead, are mixed.

[0065] As shown in drawing 3 , in the position which counters TFT30 for pixel switching respectively, shading film 11a is respectively prepared between the TFT array substrate 10 and each TFT30 for pixel switching. Shading film 11a consists of a metal simple substance containing at least one of Ti, Cr, W, Ta, Mo, and Pd which are a desirable opaque refractory metal, an alloy, metal silicide, etc. If constituted from such a material, shading film 11a is destroyed by high temperature processing in the formation process of TFT30 for pixel switching performed after the formation process of shading film 11a on the TFT array substrate 10, or it can avoid fusing by it. Since shading film 11a is formed, the situation in which the return light from the TFT array substrate 10 side etc. carries out incidence to field 1a' for channel formation of TFT30 for pixel switching or the LDD fields 1b and 1c can be prevented, and the property of TFT30 for pixel switching does not deteriorate by generating of a photocurrent.

[0066] Furthermore, between shading film 11a and two or more TFT30 for pixel switching, insulator layer 12' is prepared between the 1st layer which consists of a monolayer or a multilayer. Between the 1st layer, insulator layer 12' is prepared in order to carry out the electric insulation of the semiconductor layer 1a which constitutes TFT30 for pixel switching from shading film 11a. Furthermore, insulator layer 12' also has a function as a ground film for TFT30 for pixel switching by being formed all over the TFT array substrate 10 between the 1st layer. That is, it has the function to prevent degradation of the property of TFT30 for pixel switching with the dry area at the time of surface lapping of the

TFT array substrate 10, the dirt which remains after washing.

[0067] As shown in drawing 4 and drawing 5 especially here, between the 1st layer, the field in which capacity line 3b on the TFT array substrate 10 is formed becomes depressed in a concave compared with other fields, and insulator layer 12' is formed. Like the after-mentioned, between the 1st layer, insulator layer 12' may be constituted from a monolayer portion and a two-layer portion, and may consist of only monolayers.

[0068] Such insulator layer 12between 1st layer' consists of high insulation glass, such as NSG (non doped silicate glass), PSG (phosphorus silicate glass), BSG (boron silicate glass), and BPSG (boron phosphorus silicate glass), or a silicon-oxide film, a silicon nitride film, etc.

[0069] Between the 1st layer constituted like the above, by insulator layer 12', while being able to carry out the electric insulation of the TFT30 grade for pixel switching from shading film 11a, the situation where shading film 11a pollutes the TFT30 grade for pixel switching can be prevented. While especially insulator layer 12' is become depressed and formed in a concave here in the field to which capacity line (2nd storage-capacitance electrode) 3b was formed in the bottom of data-line 6a between the 1st layer (refer to drawing 4) it becomes depressed and forms in a concave in the field in which capacity line 3b was formed along with scanning-line 3a -- having (referring to drawing 5) -- According to the depth of the portion which became depressed in the concave as compared with the case where form an insulator layer level between the 1st layer like before, and capacity line 3b is formed on it, the difference of the sum total thickness of the field in which this capacity line 3b was formed, and the field which is not formed decreases, and flattening in the pixel section is promoted.

[0070] In drawing 4 For example, shading film (3rd storage-capacitance electrode) 11a on insulator layer 12between 1st layer', If the depth of the portion which became depressed in the concave is set up so that it may become equal to the sum total thickness of the 1f of the 1st storage-capacitance electrodes installed from drain field 1e of semiconductor layer 1a, the insulator layer 2 for capacity formation (gate insulator layer), capacity line 3b, and data-line 6a Between the 3rd layer, since the upper surface of an insulator layer 7 becomes flat, subsequent flattening processing is omissible. Or if it hollows to a concave somewhat, the burden of subsequent flattening processing is mitigable. The 1f of the 1st storage-capacitance electrodes which similarly were installed between the 1st layer in drawing 5 from drain field 1e of shading film 11a on insulator

layer 12', and semiconductor layer 1a, If the depth of the portion which became depressed in the concave is set up so that it may become equal to the sum total thickness of the insulator layer 2 for capacity formation, capacity line 3b, and data-line 6a, the upper surface of an insulator layer 7 will become almost flat between the 3rd layer (only the part of data-line 6a becomes lower than the pixel section). However, in drawing 4 and drawing 5 , insulator layer 12' may be become depressed and formed in a concave between the 1st layer in the depth corresponding to shading film 11a, the 1f of the 1st storage-capacitance electrodes, the insulator layer 2 for capacity formation, and the sum total thickness of capacity line 3b. Thus, if insulator layer 12' is constituted between the 1st layer, in drawing 5 , it will become flat [the upper surface of an insulator layer 7] between the 3rd layer, and will become almost flat in drawing 4 (only the part of data-line 6a becomes higher than the pixel section).

[0071] Moreover, especially with the gestalt of this operation, as shown in drawing 5 , let the direction of rubbing to the orientation film on pixel electrode 9a formed on the TFT array substrate 10 be the direction which met the capacity line 3b side from the scanning-line 3a side at other data-line 6a to scanning-line 3a of a couple and capacity line 3b which were put in order adjacently. It has become clear as a result of research according [that it is difficult to perform rubbing processing good to the level difference to which it is carried out by rubbing processing comparatively good to the level difference to which a field becomes high in the direction of rubbing when using the rotation rubbing method generally / here /, and a field becomes low in the direction of rubbing] to this invention person. Then, if it is made to perform rubbing processing in the direction towards the capacity line 3b side which gave flattening like the gestalt of this operation from the scanning-line 3a side which has not given flattening, since the level difference S1 in one edge of scanning-line 3a by the side of the pixel located in the upstream of the direction of rubbing turns into a level difference to which a field becomes high in the direction of rubbing, orientation restraining force will be strong and rubbing processing will be performed good. On the other hand, since the level difference S2 in the edge of another side of scanning-line 3a of the side which adjoins capacity line 3b turns into a level difference to which a field becomes low in the direction of rubbing, orientation restraining force is weak and rubbing processing is not performed good. However, while the field (small level difference S3) which is located above capacity line 3b and by which flattening was carried out is between this level

difference S2 and the pixel located in the lower stream of a river of the direction of rubbing, since it is covered collectively, it is distantly [from an opening field] separated [from the level difference S2] of scanning-line 3a of these couples, and capacity line 3b with the one band section of the shading layer 23. for this reason, the thing for which the poor orientation of the liquid crystal by this influences a picture even if rubbing processing is not performed good in a level difference S2 -- most -- or there is completely nothing Temporarily, if the direction of rubbing processing is carried out reversely, you have to narrow an opening field by the poor orientation of the liquid crystal by the level difference S1 to which a field becomes low in the direction of rubbing affecting a picture, or covering such a portion in the shading layer 23 further. Therefore, what is necessary is just to prepare capacity line 3b in an opposite side to scanning-line 3a in drawing 5 in such a case.

[0072] Furthermore, since rubbing processing is performed in this way, when carrying out rubbing of it especially along with the data line, if the scanning-line reversal drive method (1H reversal drive method) which reverses the polarity of the voltage impressed to the ends of liquid crystal for every scanning line is used since degradation of liquid crystal is not produced by direct-current drive, and in order to prevent the flicker of a display image, it is advantageous [the gestalt of this operation]. That is, generally the poor orientation (disclination) of liquid crystal tends to occur with the level difference of the pixel section in near the scanning line which is a level difference of the direction of the data line.

[0073] Here, the disclination under the influence of the horizontal electric field in TN liquid crystal is explained with reference to drawing 7 about various drive methods as an example with the poor orientation of such liquid crystal. Drawing 7 sequentially from a top A DOT (pixel) reversal drive method, 1H (line) reversal drive method, About 1S (train) reversal drive method and 1V (frame) reversal drive method The situation of the disclination in four pixel opening fields surrounded by the three scanning lines and the three data lines is shown. The right column shows especially the left column about counterclockwise TN liquid crystal by the display of the liquid crystal equipment which looked at the situation of the disclination about clockwise TN liquid crystal from the opposite substrate side. In addition, at drawing 7 , the lower right is shown for the field which the lower left is shown for the field which disclination generates by horizontal electric field in the slash section of **, in addition poor orientation generates with the level difference of the data line by the slash section of **. Moreover, suppose that the direction of

rubbing to the orientation film on a TFT array substrate is the direction of [from drawing Nakashita / upper] in this example.

[0074] As shown in drawing 7 , in the narrow field in alignment with right and left of the data line, the poor orientation of the liquid crystal by the level difference of the data line has occurred, without asking left-handed-rotation right-handed rotation. And in the case of a DOT reversal drive method, in (refer to the best stage among drawing), and left-handed-rotation liquid crystal, the disclination by horizontal electric field has occurred each scanning-line top and on the right-hand side of each data line, and the disclination by horizontal electric field has occurred in right-handed-rotation liquid crystal each scanning-line top and on the left-hand side of each data line. On the other hand, in the case of 1S reversal drive method (method which reverses the polarity of the voltage impressed to the ends of liquid crystal per data line), in (refer to the 3rd step from the inside of drawing, and a top), and left-handed-rotation liquid crystal, the disclination by horizontal electric field has occurred slightly on the right-hand side of each data line, and the disclination by horizontal electric field has occurred slightly on the left-hand side of each data line in right-handed-rotation liquid crystal. And in the case of 1V reversal drive method (method which reverses the polarity of the voltage impressed to the ends of liquid crystal for every frame or vertical-scanning period), the disclination by (referring to the bottom among drawing) and horizontal electric field is hardly generated in the upper and lower sides of the scanning line.

[0075] On the other hand, the disclination by horizontal electric field has occurred with each scanning-line up side, without asking (refer to the 2nd step from the inside of drawing, and a top), and right-handed-rotation left-handed rotation in the case of 1H reversal drive method. Therefore, as shown in drawing 7 , the direction of rubbing of the orientation film on a TFT array substrate is carried out in the direction of [on a lower shell]. If it constitutes so that the level difference of the scanning line may be located between these capacity line and the scanning line while putting in order and forming a capacity line in the field of the scanning-line top which the disclination by horizontal electric field generates The disclination by horizontal electric field will mainly be generated between this capacity line and scanning line, and the bad influence to the pixel opening field will be reduced. Furthermore, it turns out that the poor orientation of the liquid crystal which appears along with the data line by carrying out flattening of the data-line portion from drawing 7 in every reversal

drive method can be reduced.

[0076] Then, the level difference of the direction of data-line 6a consists of gestalten of this operation so that it may come between scanning-line 3a of not the edge of scanning-line 3a of a couple, and capacity line 3b but this couple, and capacity line 3b. Therefore, when a scanning-line reversal drive method (1H reversal drive method) is adopted, it will occur in the field in which the poor orientation of liquid crystal is near the center of the pixel border area covered in the shading layer 23, namely, it separated from each pixel opening field. Consequently, according to the gestalt of this operation, when a scanning-line reversal drive method is used, the influence the poor orientation of the liquid crystal in alignment with scanning-line 3a which occurs with voltage inversion affects a display image can be reduced, and raise in contrast and highly minute-ization can be attained.

[0077] As mentioned above, between the 1st layer which is needed by preparing shading film 11a, since the predetermined field of insulator layer 12' is become depressed and formed in the concave, according to the gestalt of this operation, processes, such as formation of an insulator layer by the application by the spin coat of a flattening film of the former mentioned above etc. by which flattening was carried out, can be skipped or simplified.

[0078] With the gestalt of this operation, as shown in drawing 1 and drawing 4 , high concentration drain field 1e of semiconductor layer 1a is installed along with data-line 6a, and let it be the 1f (semiconductor layer) of the 1st storage-capacitance electrodes. Therefore, a storage capacitance is first formed through the insulator layer 2 for capacity formation between the 1f (semiconductor layer) of this 1st storage-capacitance electrode, and capacity line (2nd storage-capacitance electrode) 3b. In addition, since shading film 11a is prepared also in the bottom of the 1f of the 1st storage-capacitance electrodes installed in the bottom of this data-line 6a (semiconductor layer), capacity is formed through insulator layer 12' between the 1st layer also between the 1f (semiconductor layer) of these 1st storage-capacitance electrodes, and shading film 11a.

[0079] On the other hand, as shown in drawing 1 and drawing 5 , high concentration drain field 1e of semiconductor layer 1a is installed in parallel with scanning-line 3a, and let it be the 1f (semiconductor layer) of the 1st storage-capacitance electrodes. Therefore, a storage capacitance is first formed through the insulator layer 2 for capacity formation between the 1f (semiconductor layer) of this 1st storage-capacitance electrode, and capacity line (2nd storage-capacitance electrode) 3b. In

addition, since shading film 11a is prepared also in the bottom of the 1f of this 1st storage-capacitance electrode (semiconductor layer), capacity is formed through insulator layer 12' between the 1st layer between the 1f (semiconductor layer) of these 1st storage-capacitance electrodes, and shading film (3rd storage-capacitance electrode) 11a.

[0080] The storage capacitance of pixel electrode 9a can be increased these results, using effectively the space which separated from the field under data-line 6a, and an opening field called a field parallel to the data line.

[0081] As the form of this operation shows to drawing 1 , drawing 4 , and drawing 5 , and insulator layer 12' between the 1st layer Since it is become depressed and formed in the concave in the field to which such capacity is made, flattening is attained. Furthermore, since thickness in the field which became depressed in the concave of insulator layer 12between 1st layer as this insulator layer for capacity formation' is constituted very thinly (to for example, about 1000-5000A) The capacity between shading film 11a and the 1f of the 1st storage-capacitance electrodes by which opposite arrangement was carried out through insulator layer 12' can be increased between the 1st layer concerned, without increasing the surface area of capacity line 3b. Thus, since a storage capacitance can be made to increase so that a pixel opening field may not be narrowed, and so that the flat nature of the pixel section may not be injured, the form of this operation is very advantageous.

[0082] With the form of this operation, since electrical installation of the shading film 11b (and shading film 11a in the pixel section connected to this) of the shading wiring section is carried out to constant potential line 6b as shown in drawing 2 and drawing 6 , let shading film 11a be constant potential. Therefore, potential change of shading film 11a does not have a bad influence on shading film 11a to TFT30 for pixel switching by which opposite arrangement is carried out. In this case, as constant potential of constant potential line 6b, it may be equal to grounding potential and may be equal to the potential of a counterelectrode 21. Moreover, constant potential line 6b may be connected to constant sources of potential, such as a negative supply of the circumference circuit for driving liquid crystal equipment 100, and a positive supply.

[0083] In addition, with the form of this operation, insulator layer 12' is not hollowed by the concave between the 1st layer in the field which counters TFT30 for pixel switching, or the field which counters scanning-line 3a. For this reason, if the thickness in the field which has not become depressed in a concave is set as sufficient value even if it makes

insulator layer 12' very thin in the field which became depressed in the concave between the 1st layer, the potential of shading film 11b will have a bad influence on field 1a' for channel formation of TFT30 for pixel switching, or there will be no fault which a parasitic capacitance attaches between scanning-line 3a and shading film 11b. That is, since a bad influence will not be done to TFT30 for pixel switching, or scanning-line 3a for the increase in a storage capacitance of the thickness in the field which became depressed in the concave of insulator layer 12' between the 1st layer even if it forms very thinly if the composition like the form of this operation is taken, it is very advantageous.

[0084] As shown in drawing 2 and drawing 6 , furthermore, insulator layer 12' between the 1st layer Since it is become depressed and formed in the concave in the position where shading film 11b and constant potential line 6b are connected The process which punctures contact hole 5b by etching after insulator layer 12' formation between the 1st layer like the after-mentioned becomes easy according to the depth of the portion which became depressed in this concave, and can puncture contact holes 5a and 5b collectively. Therefore, since the photolithography process and etching process only for puncturing contact hole 5b are reducible, the number of processes is not made to increase and the fall of the yield is not caused.

[0085] It sets to drawing 3 again. TFT30 for pixel switching It has LDD (Lightly Doped Drain) structure. Field 1for channel formation a' of semiconductor layer 1a in which a channel is formed of the electric field from scanning-line 3a (gate electrode) and scanning-line 3a, The gate insulator layer 2, low concentration source field (source side LDD field) 1b of semiconductor layer 1a which insulate scanning-line 3a and semiconductor layer 1a, It has high concentration source field 1e of low concentration drain field (drain side LDD field) 1c of data-line 6a (source electrode) and semiconductor layer 1a, and semiconductor layer 1a, and high concentration drain field 1e of the polysilicon contest layer 1. One to which it corresponds of two or more pixel electrode 9a is connected to high concentration drain field 1e. The source fields 1b and 1d and the drain fields 1c and 1e are formed by doping the dopant the object for n types of predetermined concentration, or for p types to semiconductor layer 1a like the after-mentioned according to whether n type or a p type channel is formed. TFT of an n type channel has the advantage that a working speed is quick, and it is used in many cases as TFT30 for pixel switching which is the switching element of a pixel. Data-line 6a (source electrode) is

constituted from the thin film of shading nature, such as alloy films, such as metal membrane metallurgy group silicide, such as aluminum, by especially the form of this operation. Moreover, between scanning-line 3a (gate electrode), the gate insulator layer 2, and the 1st layer, on insulator layer 12', while [the 2nd layer] the contact hole 8 which leads to contact hole 5a and high concentration drain field 1e which lead to 1d of high concentration source fields was formed respectively, the insulator layer 4 is formed. Electrical installation of the data-line 6a (source electrode) is carried out to 1d of high concentration source fields through contact hole 5a to this source field 1b. Furthermore, between data-line 6a (source electrode) and the 2nd layer, on the insulator layer 4, while [the 3rd layer] the contact hole 8 to high concentration drain field 1e was formed, the insulator layer 7 is formed. Electrical installation of the pixel electrode 9a is carried out to high concentration drain field 1e through the contact hole 8 to this high concentration drain field 1e. The above-mentioned pixel electrode 9a is prepared in the upper surface of an insulator layer 7 between the 3rd layer constituted in this way.

[0086] the offset structure which does not drive impurity ion into low concentration source field 1b and low concentration drain field 1c although TFT30 for pixel switching has LDD structure as mentioned above preferably -- you may have -- gate electrode 3a -- a mask -- carrying out -- high concentration -- impurity ion -- devoting oneself -- self -- you may be self aryne type TFT which forms the high concentration source and a drain field conformably

[0087] Moreover, although considered as the single-gate structure which has accepted and arranged the gate electrode (data-line 3a) of TFT30 for pixel switching between [one] source-drain field 1b and 1e with the form of this operation, you may arrange two or more gate electrodes among these. Under the present circumstances, to each gate electrode, the same signal is made to be impressed. Thus, if TFT is constituted above the dual gate (double-gate), the leakage current of a channel and a source-drain field joint can be prevented, and the current at the time of OFF can be reduced. If at least one of these gate electrodes is made into LDD structure or offset structure, the OFF state current can be reduced further and the stable switching element can be obtained.

[0088] Generally here polysilicon contest layers, such as field 1for channel formation a' of semiconductor layer 1a, and low concentration source field 1b, low concentration drain field 1c Although a photocurrent will occur according to the photo-electric-translation effect which contest polysilicon has and the transistor characteristics of TFT30 for pixel

switching will deteriorate if light carries out incidence Since data-line 6a (source electrode) is formed from the metal thin film of shading nature, such as aluminum, with the form of this operation so that scanning-line 3a (gate electrode) may be covered from the bottom The incidence of the incident light (namely, drawing 3 light from a top) to field 1for channel formation a' of semiconductor layer 1a and the LDD fields 1b and 1c can be prevented effectively at least. Moreover, as mentioned above, to the TFT30 down side for pixel switching, since shading film 11a is prepared, the incidence of the return light (namely, drawing 3 light from the bottom) to field 1for channel formation a' of semiconductor layer 1a and the LDD fields 1b and 1c can be prevented effectively at least.

[0089] In addition, in drawing 6 , insulator layer 12' consists of two insulator layers 12 and 13 between the 1st layer. Such composition is explained in full detail in the place of a manufacturing process.

[0090] (Gestalt of operation of the 2nd of liquid crystal equipment) The gestalt of operation of the 2nd of the liquid crystal equipment by this invention is explained based on drawing 8 and drawing 9 . Shading film 11a is not prepared in the TFT array substrate 10 side, but the gestalt of the 2nd operation differs from the gestalt of the 1st operation in that insulator layer 12' is further formed in the concave by becoming depressed between the 1st layer only in the field in which capacity line 3b was formed in the bottom of data-line 6a. In addition, it cannot be overemphasized that shading film 11a may be prepared as shown in drawing 1 . Drawing 8 is the plan of a TFT array substrate with which the data line, the scanning line, the pixel electrode, etc. were formed. Moreover, drawing 9 is the B-B' cross section of drawing 8 . In addition, in order to make each class and each part material into the size of the grade which can be recognized on a drawing, scales are made to have differed for each class or every each part material in drawing 9 . Moreover, the reference mark same about the same component as the gestalt of the 1st operation is attached, and the explanation is omitted.

[0091] In the field surrounded in drawing 8 by the thick line by which capacity line 3b was formed in the bottom of data-line 6a As shown in drawing 9 , insulator layer 12' is become depressed and formed in the concave between the 1st layer, and in the field corresponding to the other capacity line 3b, pixel electrode 9a, and scanning-line 3a, insulator layer 12' is mostly formed relatively between the 1st layer convex (to plane).

[0092] Therefore, since flattening only of the field where the poor orientation of only the field which a level difference produces most between the 3rd layer on the upper surface of an insulator layer 7,

i.e., liquid crystal, becomes a problem most is carried out by the concave hollow of insulator layer 12' between the 1st layer when flattening processing is not performed at all like the gestalt of this operation, the efficiency of flattening on the basis of the cost and time and effort concerning flattening processing is very good.

[0093] Moreover, insulator layer 12' is the same as that of the case of the gestalt of the 1st operation between the 1st layer shown in drawing 9 . You may constitute from a monolayer portion and a two-layer portion, and may constitute only from a monolayer.

[0094] As the gestalt of this operation shows to drawing 9 , high concentration drain field 1e of semiconductor layer 1a Since it is installed along with data-line 6a and considers as the 1f (semiconductor layer) of the 1st storage-capacitance electrodes, capacity is formed through insulator layer 12' between the 1st layer between the 1f (semiconductor layer) of the 1st storage-capacitance electrodes and capacity line (2nd storage-capacitance electrode) 3b which were installed along with data-line 6a. And flattening is attained in the field to which such a capacity is made.

[0095] (Form of operation of the 3rd of liquid crystal equipment) The form of operation of the 3rd of the liquid crystal equipment by this invention is explained based on drawing 10 . The form of the 3rd operation differs from the form of the 1st operation in that shading film 11a is not prepared in the TFT array substrate 10 side. Drawing 10 is the cross section of the liquid crystal equipment in the position corresponding to the C-C' cross section of drawing 1 . In addition, in order to make each class and each part material into the size of the grade which can be recognized on a drawing, scales are made to have differed for each class or every each part material in drawing 10 . Moreover, the reference mark same about the same component as the form of the 1st operation is attached, and the explanation is omitted.

[0096] As shown in drawing 10 , shading film 11a is not prepared as compared with drawing 5 the liquid crystal equipment of the form of the 3rd operation indicated the form of the 1st operation to be. Since it is the same as that of the form of the 1st operation about other composition, explanation is omitted.

[0097] Moreover, between the 1st layer shown in drawing 10 , like the case of the form of the 1st operation, insulator layer 12' may be constituted from a monolayer portion and a two-layer portion, and may consist of only monolayers.

[0098] Therefore, when flattening processing is not performed at all like the form of this operation, in both the field where capacity line 3b was formed in the bottom of data-line 6a which a level difference produces most, and the field in

which capacity line 3b was formed along with scanning-line 3a, flattening is attained by the concave hollow of insulator layer 12' between the 1st layer on the upper surface of an insulator layer 7 between the 3rd layer.

[0099] (Form of operation of the 4th of liquid crystal equipment) The form of operation of the 4th of the liquid crystal equipment by this invention is explained based on drawing 11 . The form of the 4th operation differs from the form of the 1st operation at the point which the TFT array substrate 10 serves as insulator layer 12between 1st layer as ground film of semiconductor layer 1a', and does not have insulator layer 12' between the 1st layer, and does not have shading film 11a. Drawing 11 is the cross section of the liquid crystal equipment in the position corresponding to the B-B' cross section of drawing 1 . In addition, in order to make each class and each part material into the size of the grade which can be recognized on a drawing, scales are made to have differed for each class or every each part material in drawing 11 . Moreover, the reference mark same about the same component as the form of the 1st operation is attached, and the explanation is omitted.

[0100] As shown in drawing 11 , as for the liquid crystal equipment of the form of the 4th operation, shading film 11a is not prepared as compared with the form of the 1st operation. Furthermore, there is no insulator layer 12' between the 1st layer, and the 1f (semiconductor layer) of the 1st storage-capacitance electrodes is formed on the direct TFT array substrate 10. And in the field in which capacity line 3b under data-line 6a was formed, the insulator layer 4 is become depressed and formed in the concave between the 2nd layer, and, thereby, flattening in the upper surface of an insulator layer 7 is attained between the 3rd layer. In addition, flattening of the insulator layer 4 may be hollowed, formed and carried out to a concave between the 2nd layer, and it is not necessary to carry out flattening like the form of the 2nd operation about the field in which capacity line 3b was formed along with scanning-line 3a.

[0101] Moreover, while [the 2nd layer] being shown in drawing 11 , an insulator layer 4 is the same as that of the case of insulator layer 12between 1st layer' in the form of the 1st operation. You may constitute from a monolayer portion and a two-layer portion, and may constitute only from a monolayer.

[0102] Thus, it is also possible to carry out flattening between the 2nd layer using an insulator layer 4.

[0103] In addition, as shown in drawing 1 , it cannot be overemphasized between shading film 11a or the 1st layer that insulator layer 12' may be prepared.

[0104] (Form of operation of the 5th of liquid crystal equipment) The form of

operation of the 5th of the liquid crystal equipment by this invention is explained based on drawing 12 . The form of the 5th operation differs from the form of the 1st operation at the point which the TFT array substrate 10 serves as insulator layer 12between 1st layer as ground film of semiconductor layer 1a', and does not have insulator layer 12' between the 1st layer, and does not have shading film 11a. Drawing 12 is the cross section of the liquid crystal equipment in the position corresponding to the B-B' cross section of drawing 1 . In addition, in order to make each class and each part material into the size of the grade which can be recognized on a drawing, scales are made to have differed for each class or every each part material in drawing 12 . Moreover, the reference mark same about the same component as the form of the 1st operation is attached, and the explanation is omitted.

[0105] As shown in drawing 12 , as for the liquid crystal equipment of the form of the 4th operation, shading film 11a is not prepared as compared with the form of the 1st operation. Furthermore, there is no insulator layer 12' between the 1st layer, and the 1f (semiconductor layer) of the 1st storage-capacitance electrodes is formed on the direct TFT array substrate 10. And in the field in which capacity line 3b under data-line 6a was formed, the insulator layer 7 is become depressed and formed in the concave between the 3rd layer, and, thereby, flattening in the upper surface of an insulator layer 7 is attained between the 3rd layer. In addition, flattening of the insulator layer 7 may be hollowed, formed and carried out to a concave between the 3rd layer, and it is not necessary to carry out flattening like the form of the 2nd operation about the field in which capacity line 3b was formed along with scanning-line 3a.

[0106] Moreover, while [the 3rd layer] being shown in drawing 12 , an insulator layer 7 is the same as that of the case of insulator layer 12between 1st layer' in the form of the 1st operation. You may constitute from a monolayer portion and a two-layer portion, and may constitute only from a monolayer.

[0107] Thus, it is also possible to carry out flattening between the 3rd layer using an insulator layer 7.

[0108] In addition, as shown in drawing 1 , it cannot be overemphasized between shading film 11a or the 1st layer that insulator layer 12' may be prepared.

[0109] (The whole liquid crystal equipment composition) The whole form composition of each operation of the liquid crystal equipment constituted as mentioned above is explained with reference to drawing 13 and drawing 14 . In addition, drawing 13 is the plan which looked at the TFT array substrate 10 from the opposite substrate 20 side with each component formed on it, and

drawing 14 is an H-H' cross section of drawing 13 shown including the opposite substrate 20.

[0110] In drawing 13 , on the TFT array substrate 10, the sealant 52 is formed along the edge and the circumference abandonment 53 of the shading nature which consists of material which is the same as the shading layer 23, or is different is formed in parallel to the inside. The data-line drive circuit 101 and the mounting terminal 102 are formed in the field of the outside of a sealant 52 along with one side of the TFT array substrate 10, and the scanning-line drive circuit 104 is established in it along with two sides which adjoin this one side. If the scanning signal delay supplied to scanning-line 3a does not become a problem, the scanning-line drive circuit 104 cannot be overemphasized by the thing only with sufficient one side. Moreover, you may arrange the data-line drive circuit 101 on both sides along the side of a screen-display field. For example, data-line 6a of an odd number train supplies a picture signal from the data-line drive circuit arranged along one side of a screen-display field, and you may make it the data line of an even number train supply a picture signal from the data-line drive circuit arranged along the side of the opposite side of the aforementioned screen-display field. Thus, if it is made to drive data-line 6a in the shape of a ctenidium, since the occupancy area of a data-line drive circuit is extensible, it becomes possible to constitute a complicated circuit. Furthermore, two or more wiring 105 for connecting between the scanning-line drive circuits 104 established in the both sides of a screen-display field is formed in one side in which the TFT array substrate 10 remains. Moreover, in at least one place of the corner section of the opposite substrate 20, the fish eye 106 which consists of flow material for taking an electric flow between the TFT array substrate 10 and the opposite substrate 20 is formed. And as shown in drawing 14 , the opposite substrate 20 with the almost same profile as the sealant 52 shown in drawing 13 has fixed to the TFT array substrate 10 by the sealant 52 concerned.

[0111] Electrical installation of the data-line drive circuit 101 and the scanning-line drive circuit 104 is respectively carried out to data-line 6a (source electrode) and scanning-line 3a (gate electrode) by wiring. The picture signal changed into the form in which a real time display is possible from the control circuit which is not illustrated is inputted into the data-line drive circuit 101, and the data-line drive circuit 101 sends the signal level according to the picture signal to it at data-line 6a (source electrode) according to the scanning-line drive circuit 104 sending a gate voltage to scanning-line 3a in order in pulse. It is

also possible to form the complementary type TFT which is the same process mostly and constitutes the data-line drive circuit 101 and the scanning-line drive circuit 104 especially from a form of this operation at the time of formation of TFT30 for pixel switching since TFT30 for pixel switching is p-Si (contest polysilicon) type TFT, and it is advantageous on manufacture.

[0112] Next, the two-dimensional layout on the TFT array substrate 100 of shading film 11b which makes the shading wiring section in the gestalt of the 1st operation to drawing 15 is shown.

[0113] As shown in drawing 15 , shading film 11a is taken about so that scanning-line 3a, capacity line 3b, and data-line 6a may be covered in the screen-display field in the circumference abandonment 53, and it is the outside of a screen-display field, it wires so that it may pass along the lower part of the circumference abandonment 53 on the opposite substrate 20, and as shown in drawing 2 , it is connected to a constant potential line. Thus, if it wires, the dead space under the circumference abandonment 53 can be used effectively, and a large area which stiffens a sealant can be taken. Moreover, the circumference abandonment 53 prepared on the opposite substrate 20 is formed with this material by shading film 11a and this layer on the TFT array substrate 10, and you may make it connect with the shading films 11a and 11b electrically. Thus, since the need becomes that there is nothing by building in the circumference abandonment 53 as for the shading layer on the opposite substrate 20, the precision at the time of the lamination of TF array substrate 10 and the opposite substrate 20 can be disregarded, and the bright liquid crystal equipment with which permeability does not vary can be realized.

[0114] In addition, you may form the inspection circuit for inspecting the quality of the precharge circuit which precedes the precharge signal of a predetermined voltage level with a picture signal, and supplies it respectively on the TFT array substrate 10 in drawing 15 at further two or more data-line 6a from drawing 13 , the sampling circuit which samples a picture signal and is respectively supplied to two or more data-line 6a, and the liquid crystal equipment concerned at the manufacture middle or the time of shipment, a defect, etc. Moreover, you may make it connect with LSI for a drive mounted on TAB (tape automated bonding substrate) instead of forming the data-line drive circuit 101 and the scanning-line drive circuit 104 on the TFT array substrate 10 electrically and mechanically through the anisotropy electric conduction film prepared in the periphery of the TFT array substrate 10.

[0115] Moreover, although not shown in

drawing 15 from drawing 1 , according to the exception of modes of operation, such as TN (Twisted Nematic) mode, STN (super TN) mode, and D-STN (double-STN) mode, and the normally white mode / normally black mode, a polarization film, a phase contrast film, a polarizing plate, etc. are respectively arranged in a predetermined direction at the side in which the outgoing radiation light of the side in which the incident light of the opposite substrate 20 carries out incidence, and the TFT array substrate 10 carries out outgoing radiation.

[0116] Next, operation of the gestalt of this operation constituted as mentioned above is explained with reference to drawing 15 from drawing 3 and drawing 13 .

[0117] First, the data-line drive circuit 101 which received the picture signal from the control circuit impresses a signal level to data-line 6a (source electrode) in the timing and the size according to this picture signal, in parallel to this, the scanning-line drive circuit 104 impresses a gate voltage to scanning-line 3a (gate electrode) one by one in pulse to predetermined timing, and TFT30 for pixel switching drives it. In TFT30 for pixel switching to which source voltage was impressed by this when the gate voltage was set to ON, voltage is impressed to pixel electrode 9a through the channel and the drain fields 1c and 1e which were formed in field 1for channel formation a[of the source fields 1d and 1b and semiconductor layer 1a]'. And as for the voltage of this pixel electrode 9a, only the time when no less than 3 figures are longer than the time when source voltage was impressed is held by the storage capacitance (refer to drawing 4 and drawing 5).

[0118] As mentioned above, if voltage is impressed to pixel electrode 9a, the orientation state of the liquid crystal in the portion pinched by this pixel electrode 9a and counterelectrode 21 in the liquid crystal layer 50 changes, and if it is a normally white mode According to the impressed voltage, passage of this liquid crystal portion of an incident light is made impossible, if it is normally black mode, according to the impressed voltage, passage of this liquid crystal portion of an incident light will be enabled, and light with the contrast according to the picture signal will carry out outgoing radiation from liquid crystal equipment 100 as a whole.

[0119] Especially, with the gestalt of this operation, since flattening in the pixel section is attained by hollowing and forming a layer insulation film in a concave, especially the poor orientation of liquid crystal is reduced near the field in which the capacity line was formed, and it becomes possible [displaying a picture high-definition by high contrast] with liquid crystal equipment 100.

[0120] Since the liquid crystal equipment 100 explained above is applied to an electrochromatic display projector, the liquid crystal equipment 100 of three sheets will be respectively used as a light valve for RGB, and incidence of the light of each color respectively decomposed through the dichroic mirror for RGB color separation will be respectively carried out to each panel as an incident light. Therefore, with the gestalt of each operation, the light filter is not prepared in the opposite substrate 20. However, you may form the light filter of RGB in the predetermined field which counters pixel electrode 9a in which the shading layer 23 is not formed in liquid crystal equipment 100 on the opposite substrate 20 with the protective coat. If it does in this way, the liquid crystal equipment of the gestalt of this operation is applicable to electrochromatic display equipments, such as direct viewing types other than a liquid crystal projector, and reflected type electrochromatic display television. Furthermore, you may form a micro lens so that it may correspond 1 pixel on [one] the opposite substrate 20. If it does in this way, bright liquid crystal equipment is realizable by improving the condensing efficiency of an incident light. Furthermore, you may form the die clo IKKU filter which makes a RGB color using interference of light by depositing the interference layer to which the refractive index of many layers is different on the opposite substrate 20 again. According to this opposite substrate with a die clo IKKU filter, brighter electrochromatic display equipment is realizable.

[0121] Although [liquid crystal equipment 100] incidence of the incident light is carried out from the opposite substrate 20 side as usual, when shading film 11a is prepared like the gestalt of the 1st operation, incidence of the incident light is carried out from the TFT array substrate 10 side, and it may be made to carry out outgoing radiation from the opposite substrate 20 side. That is, even if it attaches liquid crystal equipment 100 in a liquid crystal projector in this way, it is possible to be able to prevent light carrying out incidence to field 1for channel formation a' of semiconductor layer 1a and the LDD fields 1b and 1c, and to display a high-definition picture on them. Here, in order to prevent the reflection by the side of the rear face of the TFT array substrate 100 conventionally, the polarizing plate with which AR coat was carried out for acid resisting needs to be arranged separately, and AR film needed to be stuck. However, with the gestalt of the 1st operation, since [of the front face of the TFT array substrate 10, and semiconductor layer 1a] shading film 11a is formed at least between field 1for channel formation a', and the LDD fields 1b and 1c, such a polarizing plate and AR film by which AR

coat was carried out are used, or the need of using the substrate which carried out AR processing of TFT array substrate 10 itself is lost. Therefore, according to the gestalt of this operation, material cost can be cut down, and a contaminant, a blemish, etc. do not drop the yield at the time of polarizing plate attachment, and it is very advantageous. Moreover, since lightfastness is excellent, even if it uses the bright light source, or it carries out polarization conversion by the polarization beam splitter and it raises efficiency for light utilization, quality-of-image degradation of the cross talk by light etc. is not produced.

[0122] Moreover, although it was explained that the switching element of liquid crystal equipment 100 was a right stagger type or the KOPURANA type polysilicon contest TFT, the gestalt of this operation is effective also to TFT of other form, such as reverse stagger type TFT and an amorphous silicon TFT.

[0123] Furthermore, in liquid crystal equipment 100, although the liquid crystal layer 50 was constituted from a pneumatic liquid crystal as an example, if the polymer dispersed liquid crystal which distributed liquid crystal as a minute grain in the macromolecule is used, the orientation films 19 and 22 and the above-mentioned polarization film, a polarizing plate, etc. will become unnecessary, and the advantage of a raise in the brightness of liquid crystal equipment or low-power-izing by efficiency for light utilization increasing will be acquired. Furthermore, when applying liquid crystal equipment 100 to reflected type liquid crystal equipment by constituting pixel electrode 9a from a metal membrane with high reflection factors, such as aluminum, you may use SH (super HOMEOTORO pick) type liquid crystal to which perpendicular orientation of the liquid crystal molecule was mostly carried out in the state of no voltage impressing. Furthermore, although the counterelectrode 21 is provided in the opposite substrate 20 side in liquid crystal equipment 100 again so that perpendicular electric field (vertical electric field) may be impressed to the liquid crystal layer 50 What (that is, the electrode for horizontal electric-field generating is prepared in the TFT array substrate 10 side, without preparing the electrode for vertical electric-field generating in the opposite substrate 20 side) pixel electrode 9a is respectively constituted also for from an electrode for horizontal electric-field generating of a couple so that electric field (horizontal electric field) parallel to the liquid crystal layer 50 may be impressed is possible. Thus, it is advantageous, when extending an angle of visibility rather than the case where vertical electric field are used, if horizontal electric field are used. In addition, it is possible to apply the gestalt of this operation to various kinds of liquid

crystal material (liquid crystal phase), a mode of operation, a liquid crystal array, the drive method, etc.

[0124] (Manufacture process) Next, it is explained with reference to drawing 23 from drawing 16 , using the liquid crystal equipment of the gestalt of the 1st operation about the manufacture process of liquid crystal equipment with the above composition as an example. In addition, it is process drawing which drawing 19 is made to correspond to the B-B' cross section of drawing 4 including the characteristic part in the gestalt of the 1st operation of each class by the side of the TFT array substrate in each process from drawing 16 , and is shown, and is process drawing which drawing 23 makes each class by the side of the TFT array substrate in each process correspond to the D-D' cross section of drawing 6 from drawing 20 , and is shown further. And the process (1) described in these drawings - a process (20) are respectively put in block as the same process in the portion into which it is [on the TFT array substrate 1] different from each other, and are performed.

[0125] First, with reference to drawing 19 , it explains from drawing 16 focusing on the manufacture process of the portion which was formed in data-line 3a corresponding to the B-B' cross section of drawing 4 , and the bottom of it and which capacity line 3b Reaches and contains the 1f (semiconductor layer) of the 1st storage-capacitance electrodes. In addition, since the manufacture distance of the component shown in the A-A'C-C of manufacture distance [of the component shown in the cross section] or drawing 5 ' cross section of drawing 3 is also put in block with each distance shown in drawing 19 and is performed from drawing 16 , explanation is suitably added for every distance also about these manufacturing processes.

[0126] As shown in the process (1) of drawing 16 , the TFT array substrates 10, such as a quartz substrate and hard glass, are prepared. Here, preferably, annealing processing is carried out at inert gas atmosphere, such as N2 (nitrogen), and the elevated temperature of about 900-1300 degrees C, and it pretreats so that distortion produced in the TFT array substrate 10 in the elevated-temperature process carried out behind may decrease. That is, according to the temperature by which high temperature processing is carried out at the maximum elevated temperature in a manufacture process, the TFT array substrate 10 is heat-treated at the same temperature or the temperature beyond it in advance.

[0127] Thus, all over the processed TFT array substrate 10, about 1000-5000A thickness and the shading film 11 which is about 2000A thickness preferably are formed for metal alloy films, such as metal metallurgy group silicide, such as Ti, Cr, W, Ta, Mo, and Pd, by the spatter.

[0128] Then, as shown in a process (2), shading film 11a is formed by forming the resist mask corresponding to the pattern (referring to drawing 1) of shading film 11a by the photolithography on the this formed shading film 11, and etching to the shading film 11 through this resist mask.

[0129] As shown in a process (3), by the ordinary pressure or reduced pressure CVD on shading film 11a Next, TEOS (tetrapod ethyl orthochromatic silicate) gas, TEB (tetrapod ethyl boat rate) gas, TMOP (tetrapod methyl OKISHI force rate) gas, etc. are used. The 1st insulator layer 12 (lower layer of two-layer insulator layer 12between 1st layer') which consists of silicate glass films, such as NSG, PSG, BSG, and BPSG, a silicon nitride film, a silicon-oxide film, etc. is formed. The thickness of this 1st insulator layer 12 considers as about 5000-20000A, and determines the thickness of the 1st insulator layer 12 by the thickness of a film to embed at a next process.

[0130] Next, as shown in a process (4), to the field (refer to drawing 1 , drawing 4 , and drawing 5) which is due to form capacity line 3b up, it etches and the 1st insulator layer 12 in this field is removed. Here, since the 1st insulator layer 12 can be removed in different direction in the almost same size as the resist mask formed by the photolithography when the aforementioned etching is processed by dry etching, such as reactant etching and reactant ion beam etching, there is an easily controllable advantage as a design size. Although the puncturing field of the 1st insulator layer 12 spreads on the other hand since it is isotropic when wet etching is used as it is also few, since the side-attachment-wall side of an aperture can be formed in the shape of a taper, the polysilicon contest film 3 or resist for forming scanning-line 3a of a back process do not remain in the circumference of a side attachment wall of an aperture, without etching and exfoliating, and do not cause the fall of the yield. In addition, as a method of forming the side-attachment-wall side of the aperture of the 1st insulator layer 12 in the shape of a taper, once it **********s by dry etching, a resist pattern may be retreated and dry etching may be performed again. Moreover, it cannot be overemphasized that dry etching and wet etching may be combined.

[0131] Next, as shown in a process (5), the 2nd insulator layer 13 (upper layer of two-layer insulator layer 12between 1st layer') which consists of a silicate glass film, a silicon nitride film, a silicon-oxide film, etc. is formed like the 1st insulator layer 12 on shading film 11a and the 1st insulator layer 12. The thickness of this 2nd insulator layer 13 may be about 1000-2000A. To the 2nd insulator layer 13, by performing about 900-degree C annealing processing, while preventing

contamination, you may carry out flattening.

[0132] Especially with the gestalt of this operation, as shown in drawing 4 , before pixel electrode 9a is formed in the field to which capacity line 3b is formed in the bottom of data-line 6a, the thickness of the 1st insulator layer 12 which forms insulator layer 12' between the 1st layer, and the 2nd insulator layer 13 is set up so that a pixel field may become flatness mostly.

[0133] Next, as shown in a process (6), about 450-550 degrees C of amorphous silicon films are preferably formed comparatively on the 2nd insulator layer 13 with the reduced pressure CVD (for example, CVD with a pressure of about 20-40Pa) using the mono-silane gas of flow rate about 400 to 600 cc/min, disilane gas, etc. of about 500 degrees C in low-temperature environment. Then, in nitrogen atmosphere, at about 600-700 degrees C, preferably, solid phase growth of the polysilicon contest film 1 is carried out by ****** which performs annealing processing of 4 - 6 hours for about 1 to 10 hours until it becomes the thickness of about 1000A preferably in about 500-2000A thickness.

[0134] Under the present circumstances, as TFT30 for pixel switching shown in drawing 3 , in creating n channel type TFT30 for pixel switching, it dopes slightly the dopant of V group elements, such as Sb (antimony), As (arsenic), and P (Lynn), with an ion implantation etc. to the field for channel formation concerned. Moreover, in using TFT30 for pixel switching as a p-channel type, it dopes slightly the dopant of III group elements, such as B (boron), Ga (gallium), and In (indium), with an ion implantation etc. In addition, you may form the polysilicon contest film 1 directly by reduced pressure CVD etc. without passing through an amorphous silicon film. Or drive silicon ion into the polysilicon contest film deposited by reduced pressure CVD etc., once make it amorphous (amorphous-izing), it is made to recrystallize by annealing processing etc. after that, and the polysilicon contest film 1 may be formed.

[0135] Next, as shown in the process (7) of drawing 17 , semiconductor layer 1a of the **** predetermined pattern shown in drawing 1 is formed according to a photolithography process, an etching process, etc. That is, the 1f (semiconductor layer) of the 1st storage-capacitance electrodes installed from semiconductor layer 1a (refer to drawing 3) which constitutes TFT30 for pixel switching is formed especially in the field in which capacity line 3b is formed along with the field in which capacity line 3b is formed, and scanning-line 3a under data-line 6a (refer to drawing 4 and drawing 5).

[0136] As shown in a process (8), the 1f (semiconductor layer) of the 1st

storage-capacitance electrodes with semiconductor layer 1a which constitutes TFT30 for pixel switching next, the temperature of about 900-1300 degrees C, and by oxidizing thermally with the temperature of about 1000 degrees C preferably Form a thermal oxidation silicon film with a comparatively thin thickness of about 300A, and a high-temperature-oxidation silicon film (HTO film) and a silicon nitride film are further deposited on the comparatively thin thickness of about 500A by reduced pressure CVD etc. The insulator layer 2 for capacity formation is formed with the gate insulator layer 2 (refer to drawing 3) of TFT30 for pixel switching with multilayer structure (refer to drawing 4 and drawing 5). consequently, the thickness of the 1f of the 1st storage-capacitance electrodes (semiconductor layer 1a) -- the thickness of about 300-1500A -- desirable -- the thickness of about 350-500A -- becoming -- the thickness of the insulator layer 2 for capacity formation (gate insulator layer) -- the thickness of about 200-1500A -- it becomes the thickness of about 300-1000A preferably Thus, by shortening elevated-temperature thermal oxidation time, when using especially an about 8 inches large-sized wafer, the warp by heat can be prevented. However, you may form the insulator layer 2 (gate insulator layer 2) for capacity formation with a single layer structure only by oxidizing the polysilicon contest layer 1 thermally.

[0137] In addition, although not limited especially in a process (8), you may make the amount of [used as the 1f of the 1st storage-capacitance electrodes] semiconductor layer dope and form for example, P ion into low resistance in about 3x1012/cm2 of doses.

[0138] Next, thermal diffusion of the process (Lynn (P as shown in 9), after depositing the polysilicon contest layer 3 by reduced pressure CVD etc.) is carried out, and the polysilicon contest film 3 is electric-conduction-ized. Or you may use the doped silicon film which introduced P ion simultaneously with membrane formation of the polysilicon contest film 3. As shown in a process (10), capacity line 3b is formed according to the photolithography process using the resist mask, an etching process, etc. with scanning-line 3a (gate electrode) of the **** predetermined pattern shown in drawing 1 . Thickness of such capacity line 3b (scanning-line 3a) is made into about 3500A.

[0139] However, capacity line 3b and scanning-line 3a may be formed from a high-melting point metal membrane or metal silicide films, such as not a polysilicon contest layer but W, Mo, etc., or may be formed in a multilayer combining these metal membranes or a metal silicide film, and a polysilicon contest film. in this case, if the shading

layer 23 arranges capacity line 3b and scanning-line 3a as the part or the shading film which boils all and corresponds of a wrap field, it will also become possible to omit a part or all of the shading layer 23 by the shading nature which a metal membrane metallurgy group silicide film has In this case, there is an advantage which can prevent decline in the pixel numerical aperture by the lamination gap with the opposite substrate 20 and the TFT array substrate 10 especially.

[0140] Next, as shown in a process (11), when TFT30 for pixel switching shown in drawing 3 is set to n channel type TFT with LDD structure, In order to form low concentration source field 1b and low concentration drain field 1c in semiconductor layer 1a first The dopant 200 of V group elements, such as P, is doped by low concentration, using scanning-line 3a (gate electrode) as a diffusion mask (with for example, dose which is one to 3x1013-/cm2 about P ion). Thereby, semiconductor layer 1a under scanning-line 3a (gate electrode) becomes field 1a' for channel formation. Capacity line 3b and scanning-line 3a are also formed into low resistance by the dope of this impurity (refer to drawing 4 and drawing 5).

[0141] Then, as shown in the process (12) of drawing 18 , in order to form high concentration source field 1b and high concentration drain field 1c which constitute TFT30 for pixel switching after forming the resist layer 202 on scanning-line 3a (gate electrode) with a mask with wide width of face rather than scanning-line 3a (gate electrode), similarly the dopant 201 of V group elements, such as P, is doped by high concentration (for example, P ion -- the dose of one to 3x1015-/cm2) Moreover, when using TFT30 for pixel switching as a p-channel type, in order to form low concentration source field 1b, low concentration drain field 1c and 1d of high concentration source fields, and high concentration drain field 1e in semiconductor layer 1a, the dopant of III group elements, such as B, is used and doped. Thus, when it considers as LDD structure, the advantage which can reduce the short channel effect is acquired. In addition, it is good also as TFT of offset structure, without, for example, performing a low-concentration dope, and it is good also as self aryne type TFT by the ion-implantation technology using P ion, B ion, etc., using scanning-line 3a (gate electrode) as a mask.

[0142] Capacity line 3b and scanning-line 3a are also further formed into low resistance by the dope of this impurity (refer to drawing 4 and drawing 5).

[0143] In parallel to these processes, the data-line drive circuit 101 and the scanning-line drive circuit 104 with the complementary-type structure which

consists of n channel type TFT and p-channel type TFT are formed in the periphery on the TFT array substrate 10. Thus, since TFT30 for pixel switching is the polysilicon contest TFT in the form of this operation, at the time of formation of TFT30 for pixel switching, it is the same process mostly, and the data-line drive circuit 101 and the scanning-line drive circuit 104 can be formed, and it is advantageous on manufacture.

[0144] Next, using an ordinary pressure or reduced pressure CVD, TEOS gas, etc., as shown in a process (13), while [the 2nd layer] consisting of silicate glass films, such as NSG, PSG, BSG, and BPSG, a silicon nitride film, a silicon-oxide film, etc., an insulator layer 4 is formed, so that capacity line 3b and scanning-line 3a may be covered with scanning-line 3a (gate electrode) in TFT30 for pixel switching (refer to drawing 4 and drawing 5). The thickness of an insulator layer 4 has desirable about 5000-15000A between the 2nd layer.

[0145] Next, as shown in drawing 3 , in order to activate 1d of high concentration source fields, and high concentration drain field 1e, after performing about 1000-degree C annealing processing about 20 minutes in the stage of a process (14), contact hole 5a to the data line 31 (source electrode) is formed by dry etching, such as reactant etching and reactant ion beam etching. Under the present circumstances, there is an advantage that the direction which punctured contact hole 5a etc. can make a puncturing configuration almost the same as a mask configuration by anisotropic etching like reactant etching and reactant ion beam etching. However, if it punctures combining dry etching and wet etching, since these contact hole 5a etc. will be made in the shape of a taper, the advantage that the open circuit at the time of wiring connection can be prevented is acquired. Moreover, the contact hole for connecting with the wiring which illustrates neither scanning-line 3a nor capacity line 3b (refer to drawing 5) is also punctured to an insulator layer 4 between the 2nd layer according to the same process as contact hole 5a.

[0146] Next, between the 2nd layer, as shown in a process (15), as it deposits on about 3000A preferably in about 1000-5000A thickness by making low resistance metal metallurgy group silicide, such as aluminum of shading nature, etc. into a metal membrane 6 and is further shown in a process (16) by spatter processing etc., data-line 6a (source electrode) is formed according to a photolithography process, an etching process, etc. on an insulator layer 4.

[0147] Next, using an ordinary pressure or reduced pressure CVD, TEOS gas, etc., as shown in the process (17) of drawing 19 , while [the 3rd layer] consisting of silicate glass films, such as NSG, PSG,

BSG, and BPSG, a silicon nitride film, a silicon-oxide film, etc., an insulator layer 7 is formed, so that a data-line 6a (source electrode) top may be covered. The thickness of an insulator layer 7 has desirable about 5000-15000A between the 3rd layer.

[0148] Especially with the gestalt of this operation, since the insulator layer is become depressed and formed in the concave between the 1st layer of the process (4) of drawing 16 , and (5) in the field in which capacity line 3b is formed, the front face of the pixel field located above capacity line 3b in the stage which finished this process (17) becomes almost flat. In addition, in order to set to liquid crystal equipment 100 and to suppress further the poor orientation of the liquid crystal molecule by the side of the TFT array substrate 10, a flattening film may be further applied on a spin coat etc. on an insulator layer 7 between the 3rd layer, or CMP processing may be performed. Or you may form an insulator layer 7 by the flattening film between the 3rd layer. Since the portion in which the capacity line etc. was formed of the concave hollow of insulator layer 12' between the 1st layer, and the other portion are made into the almost same height with the gestalt of this operation as shown in drawing 6 etc. from drawing 4 , although such flattening processing generally is not required, in order to display a more nearly high-definition picture, when performing further flattening in the best layer in this way, a flattening film can be made very thin or flattening processing is only added slightly -- since it ends, the gestalt of this operation is very advantageous

[0149] Next, in the stage of a process (18), as shown in drawing 3 , in TFT30 for pixel switching, the contact hole 8 for carrying out electrical installation of pixel electrode 9a and the high concentration drain field 1e is formed by dry etching, such as reactant etching and reactant ion beam etching. Under the present circumstances, the advantage that the direction which punctured the contact hole 8 can make a puncturing configuration almost the same as a mask configuration by anisotropic etching like reactant etching and reactant ion beam etching is acquired. However, if it punctures combining dry etching and wet etching, since a contact hole 8 will be made in the shape of a taper, the advantage that the open circuit at the time of wiring connection can be prevented is acquired.

[0150] Next, between the 3rd layer, as shown in a process (19), as the transparent conductivity thin films 9, such as an ITO film, are deposited on the thickness of about 500-2000A and are further shown in a process (20) by spatter processing etc., pixel electrode 9a is formed according to a photolithography process, an etching process, etc. on an

insulator layer 7. In addition, when using the liquid crystal equipment 100 concerned for reflected type liquid crystal equipment, you may form pixel electrode 9a from an opaque material with high reflection factors, such as aluminum.

[0151] Then, after applying the application liquid of the orientation film of a polyimide system on pixel electrode 9a, the orientation film 19 shown in drawing 3 is formed by performing rubbing processing in the predetermined direction so that it may have a predetermined pre tilt angle etc.

[0152] On the other hand, about the opposite substrate 20 shown in drawing 3 , a glass substrate etc. is prepared first, and after the circumference abandonment 53 of the shading layer 23 and shading nature carries out the spatter for example, of the metal chromium, it is formed through a photolithography process and an etching process. In addition, the shading layer 23 and the circumference abandonment 53 may form others, carbon, and Ti, such as Cr, nickel, and aluminum, from material, such as resin black distributed to the photoresist. [metallic material]

[0153] Then, a counterelectrode 21 is formed by spatter processing etc. all over the opposite substrate 20 by depositing transparent conductivity thin films, such as ITO, on the thickness of about 500-2000A. Furthermore, after applying the application liquid of the orientation film of a polyimide system all over a counterelectrode 21, the orientation film 22 is formed by performing rubbing processing in the predetermined direction so that it may have a predetermined pre tilt angle etc.

[0154] With the gestalt of this operation, rubbing processing is performed towards going to the capacity line 3b side as mentioned above from the scanning-line 3a side which adjoined each other along with data-line 6a. since it is located near the center of the border area where the level difference S2 (refer to drawing 5) with the difficult property top rubbing processing is covered by the shading layer 23 by this, the poor orientation in this level difference S2 has a bad influence on a pixel opening field -- most -- or there is completely nothing

[0155] Finally, the liquid crystal with which the TFT array substrate 10 and the opposite substrate 20 in which each class was formed as mentioned above are stuck by the sealant 52 so that the orientation films 19 and 22 may meet, and they come to mix two or more kinds of pneumatic liquid crystals to the space between both substrates by vacuum suction etc. is attracted, and the liquid crystal layer 50 of predetermined thickness is formed.

[0156] Next, with reference to drawing 23 , the manufacture process of the portion containing a part for the connection of the shading film and the

constant potential line corresponding to the D-D' cross section of drawing 6 is explained from drawing 20 .

[0157] The process (20) of the process (1) of drawing 20 to drawing 23 is performed as the same manufacture process as the process (20) of drawing 19 from the process (1) of drawing 16 mentioned above.

[0158] That is, as shown in the process (1) of drawing 20 , after forming the shading film 11 all over the TFT array substrate 10, as shown in a process (2), shading film 11b is formed according to a photolithography process, an etching process, etc.

[0159] Next, as are shown in a process (3), and the 1st insulator layer 12 (lower layer of two-layer insulator layer 12between 1st layer') is formed on shading film 11b and it is shown in a process (4), to the field which is due to form a part for a connection up, it etches and the 1st insulator layer 12 in this field is removed. Here, since the 1st insulator layer 12 can be removed in different direction in the almost same size as the resist mask formed by the photolithography when etching is processed by dry etching, such as reactant etching and reactant ion beam etching, there is an easily controllable advantage as a design size. Although the puncturing field of the 1st insulator layer 12 spreads on the other hand since it is isotropic when wet etching is used as it is also few, since the side-attachment-wall side of an aperture can be formed in the shape of a taper, the polysilicon contest film or resist for forming for example, scanning-line 3a of a back process do not remain in the circumference of a side attachment wall of an aperture, without etching and exfoliating, and do not cause the fall of the yield. In addition, as a method of forming the side-attachment-wall side of the aperture of the 1st insulator layer 12 in the shape of a taper, once it **********s by dry etching, a resist pattern may be retreated and dry etching may be performed again.

[0160] Then, as shown in a process (5), the 2nd insulator layer 13 (upper layer of two-layer insulator layer 12between 1st layer') is formed on shading film 11b and the 1st insulator layer 12.

[0161] Next, as shown in a process (6), after forming an amorphous silicon film on the 2nd insulator layer 13, solid phase growth of the polysilicon contest film 1 is carried out.

[0162] Next, as are shown in a process (9) waiting and after that and formation of semiconductor layer 1a [in / the pixel section / at the process (7) of drawing 21 and (8)] and the gate insulator layer 2 is shown in a process (10) once depositing the polysilicon contest layer 3, in a part for this connection, the polysilicon contest layer 3 is removed altogether.

[0163] Next, as shown in the process (11) of drawing 21 , and the process (12) of

drawing 22 , the dope of the impurity ion for semiconductor layer 1a is completed.

[0164] Next, an insulator layer 4 is formed between the 2nd layer, and as shown in a process (13), as shown in a process (14), contact hole 5b for connecting shading film 11b and constant potential line 6b is opened in an insulator layer 4 between the 2nd layer, so that the 1st insulator layer 13 may be covered. Under the present circumstances, since only the 2nd insulator layer 13 is formed in the bottom of an insulator layer 4 among insulator layer 12' between the 1st layer between the 2nd layer, an insulator layer 4 is punctured between the 2nd layer on 1d of high concentration source fields of semiconductor layer 1a, and it can puncture at a stretch at the same etching process as the process (process of drawing 18 (14)) which forms contact hole 5a.

[0165] Next, between the 2nd layer, as shown in a process (15), after depositing aluminum etc. as a metal membrane 6, as it is shown in a process (16) by spatter processing etc., constant potential line 6b which consists of the same layers (aluminum etc.) as the data line is formed according to a photolithography process, an etching process, etc. on an insulator layer 4.

[0166] Next, between constant potential line 6b and the 2nd layer, as shown in the process (17) of drawing 23 , an insulator layer 7 is formed between the 3rd layer so that an insulator layer 4 top may be covered.

[0167] Next, at a process (18), as shown in a process (19), the transparent conductivity thin films 9, such as an ITO film, are once deposited on an insulator layer 7 between the 3rd layer, and after waiting to puncture the contact hole 8 shown in drawing 3 , as further shown in a process (20), about this portion, all are removed according to a photolithography process, an etching process, etc.

[0168] According to the manufacture method of the liquid crystal equipment in the form of this operation, as mentioned above as contact hole 5b for connecting shading film 11b and constant potential line 6b An insulator layer 4 and the 1st insulator layer 13 (upper layer of the insulator layer between the 1st layer) are punctured between the 2nd layer until it results in shading film 11b, and simultaneously, as contact hole 5a for connecting TFT30 for pixel switching, and data-line 6a, an insulator layer 4 is punctured between the 2nd layer until it results in semiconductor layer 1a. Therefore, since these two kinds of contact holes 5a and 5b can be punctured collectively, it is advantageous on manufacture. For example, it becomes possible to puncture two kinds of such contact holes 5a and 5b collectively by the wet etching which sets a selection ratio as a suitable value, so that it may become the predetermined depth respectively.

According to the depth of the portion which became depressed in the concave of an insulator layer between the 1st layer especially, the process which punctures these contact holes becomes easy. Since the contact hole puncturing processes (a photolithography process, etching process, etc.) for connecting a constant potential line with a shading film can be deleted, the increase of a manufacturing cost or the fall of the yield by the increase of a process are not caused.

[0169] As explained above, according to the manufacture process in the form of this operation, thickness of insulator layer 12between 1st layer' in the portion which became depressed in the concave is made comparatively easy, and can be controlled by management of the thickness of the 2nd insulator layer 13 certainly and with high precision. Therefore, it also becomes possible to make very thin thickness of insulator layer 12between 1st layer' in the portion which became depressed in this concave.

[0170] In addition, what is necessary is to add some change to the process (3) respectively shown in drawing 16 and drawing 20 , (4), and (5), and just to perform (20) from a process (1), in constituting an insulator layer 12 from a monolayer between the 1st layer. Namely, in a process (3), on shading film 11a, deposit the insulator layer 12 between the 1st layer of a monolayer [a little] thicker as it was called about 10000-15000A, and it sets at a process (4). To the field which is due to form capacity line 3b up, it etches and leaves the thickness of about 1000-2000A for the insulator layer 12 between the 1st layer in this field. And a process (5) is skipped. also in this case, the thickness of the portion into which an insulator layer 12 does not ********** between the 1st layer and etching -- the bottom, before pixel electrode 9a is formed behind, the thickness of a portion is set up so that a pixel field may become flatness mostly Thus, since flattening can be attained if the thickness of the portion which there is no need of making the number of layers increasing, and became depressed in the concave, and the portion which is not so is controlled by etching time management even if it will compare with the conventional case, if an insulator layer 12 is constituted from a monolayer between the 1st layer, it is convenient.

[0171] (Electronic equipment) Next, the form of operation of electronic equipment equipped with the liquid crystal equipment 100 explained to the detail above is explained with reference to drawing 28 from drawing 24 .

[0172] The outline composition of the electronic equipment which equipped drawing 24 with liquid crystal equipment 100 in this way is shown first.

[0173] In drawing 24 , electronic equipment is equipped with the source 1000 of a display information output, the

display information processing circuit 1002, the drive circuit 1004, liquid crystal equipment 100, the clock generation circuit 1008, and a power circuit 1010, and is constituted. The source 1000 of a display information output outputs display information, such as a picture signal of a predetermined format, to the display information processing circuit 1002 based on the clock signal from the clock generation circuit 1008 including the tuning circuit which aligns and outputs memory, such as ROM (Read Only Memory), RAM (Random Access Memory), and an optical disk unit, and a picture signal. The display information processing circuit 1002 is constituted including various well-known processing circuits, such as amplification / inversion circuit, a phase expansion circuit, a rotation circuit, a gamma correction circuit, and a clamping circuit, generates a digital signal one by one from the display information inputted based on the clock signal, and outputs it to the drive circuit 1004 with a clock signal CLK. The drive circuit 1004 drives liquid crystal equipment 100. A power circuit 1010 supplies a predetermined power supply to each above-mentioned circuit. In addition, on the TFT array substrate which constitutes liquid crystal equipment 100, the drive circuit 1004 may be carried and, in addition to this, the display information processing circuit 1002 may be carried.

[0174] Next, the example of the electronic equipment constituted in this way from drawing 25 by drawing 28 is shown respectively.

[0175] In drawing 25 , an example slack liquid crystal projector 1100 of electronic equipment prepares three liquid crystal modules containing the liquid crystal equipment 100 with which the drive circuit 1004 mentioned above was carried on the TFT array substrate, and is constituted as a projector respectively used as light valves 100R, 100G, and 100B for RGB. In a liquid crystal projector 1100, if an incident light is emitted from the lamp unit 1102 of the white light sources, such as a metal halide lamp, it will be divided into the optical components R, G, and B corresponding to the three primary colors of RGB by the mirror 1106 of three sheets, and the dichroic mirror 1108 of two sheets, and will be respectively led to the light valves 100R, 100G, and 100B corresponding to each color. Under the present circumstances, especially B light is drawn through the relay lens system 1121 which consists of the incidence lens 1122, a relay lens 1123, and an outgoing radiation lens 1124, in order to prevent the optical loss by the long optical path. And after the optical component corresponding to the three primary colors respectively modulated by light valves 100R, 100G, and 100B is again compounded with a dichroic prism 1112,

it is projected by the screen 1120 as a color picture through a projector lens 1114.

[0176] Since the shading film is prepared also in the TFT bottom especially with the form of this operation, The reflected light by the incident-light study system in the liquid crystal projector based on the incident light from the liquid crystal equipment 100 concerned, After carrying out outgoing radiation from the reflected light from the front face of the TFT array substrate at the time of an incident light passing, and other liquid crystal equipments, even if a part of incident light which runs through a dichroic prism 1112 carries out incidence from a TFT array substrate side as a return light Shading to channel fields, such as TFT for switching of a pixel electrode, can fully be performed. For this reason, in composition, since it becomes unnecessary to stick AR film for return light prevention, or to perform AR coat processing between the TFT array substrate of each liquid crystal equipment and prism at a polarizing plate even if it uses the prism suitable for the miniaturization for an incident-light study system, small and when being simplified, it is very advantageous.

[0177] In drawing 26 , other personal computers 1200 of the laptop type dealing with example slack multimedia of electronic equipment (PC) are equipped with the main part 1204 with which the keyboard 1202 was incorporated while it has liquid crystal equipment 100 mentioned above in the top covering case and they hold CPU, memory, a modem, etc. further.

[0178] In drawing 27 , the drive circuit 1004 of the above-mentioned [other example slack pagers 1300 of electronic equipment] in the metal frame 1302 is held with the light guide 1306 in which the liquid crystal equipment 100 which is carried at a TFT array substrate top and forms a liquid crystal display module contains back light 1306a, the circuit board 1308, the 1st, and 2nd shield boards 1310, 1312 or 2 elastic conductors 1314 and 1316, and the tape carrier package tape 1318. In the case of this example, the above-mentioned display information processing circuit 1002 (refer to drawing 24) may be carried in the circuit board 1308, and may be carried on the TFT array substrate of liquid crystal equipment 100. Furthermore, it is also possible to carry the above-mentioned drive circuit 1004 on the circuit board 1308.

[0179] In addition, since the example shown in drawing 27 is a pager, the circuit board 1308 grade is prepared. However, it is also possible to carry out production, sale, use, etc. as liquid crystal equipment of the back light formula which incorporated [in the case of the drive circuit 1004 or the liquid crystal equipment 100 which carries the display

information processing circuit 1002 further, and forms a liquid crystal module] the light guide 1306 by using as liquid crystal equipment what fixed liquid crystal equipment 100 in the metal frame 1302 in addition to this.

[0180] moreover, as shown in drawing 28 , in the case of the liquid crystal equipment 100 which carries neither the drive circuit 1004 nor the display information processing circuit 1002 To TCP (Tape Carrier Package)1320 mounted on the polyimide tape 1322, IC1324 including the drive circuit 1004 or the display information processing circuit 1002 It is also possible to connect physically and electrically through the anisotropy electric conduction film prepared in the periphery of the TFT array substrate 10, and to carry out production, sale, use, etc. as liquid crystal equipment.

[0181] ****** equipped with the video tape recorder of a liquid crystal television, a viewfinder type, or a monitor direct viewing type, the car navigation equipment, the electronic notebook, the calculator, the word processor, the engineering workstation (EWS), the cellular phone, the TV phone, POS terminal, and touch panel other than electronic equipment which were explained with reference to drawing 28 from drawing 25 above etc. is mentioned as an example of the electronic equipment shown in drawing 24.

[0182] As explained above, according to the form of this operation, manufacture efficiency is high and various kinds of electronic equipment equipped with the liquid crystal equipment 100 in which high-definition image display is possible by high contrast can be realized.

[0183]

[Effect of the Invention] While according to the liquid crystal equipment of this invention the space of the pixel boundary in alignment with the space and the scanning line under the data line unusable as a pixel opening field can be used effectively in order to give a storage capacitance to a pixel electrode, flattening near the pixel section located above the data line is attained, the poor orientation of the liquid crystal which was the easiest to occur near this can be reduced efficiently, and high definition image display becomes possible by high contrast. On the other hand, it is difficult to perform rubbing processing appropriately by performing rubbing processing in the predetermined direction, and if the part where the poor orientation of liquid crystal tends to occur can be arranged in the position which does not have a bad influence on image display and is put in another way, it will also become possible to raise a pixel numerical aperture efficiently. When a scanning-line reversal drive method (1H reversal drive method) is used especially, this effect shows up notably. Moreover, it

can increase efficiently in the space to which the storage capacitance of a pixel electrode was restricted by it being hollowed by the concave for flattening, therefore using a thin insulator layer portion as an insulator layer for capacity formation. Furthermore, this storage capacitance can be increased still more efficiently also using the shading film arranged to the TFT down side. Furthermore, it is also possible to make easy connection between a shading film and the constant source of potential again.

[0184] on the other hand -- according to the manufacture method of the liquid crystal equipment of this invention -- comparatively easy process control -- or according to a reliable process, although the liquid crystal equipment of this invention is manufactured, it becomes possible Moreover, it also becomes possible by making the insulator layer for capacity formation very thin to increase the storage capacitance of a pixel electrode efficiently. Furthermore, it is also possible by puncturing various kinds of contact holes collectively to attain low-cost-ization in liquid crystal equipment.

[0185] Moreover, according to the electronic equipment of this invention, deterioration of the quality of image by the poor orientation of liquid crystal is reduced, and by high contrast, high-definition image display is possible and it becomes realizable about various electronic equipment, such as a liquid crystal projector of a low cost, a personal computer, and a pager.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is the plan of a TFT array substrate with which the liquid crystal equipment in the gestalt of operation of the 1st of this invention is equipped and with which the data line, the scanning line, the pixel electrode, the shading film, etc. were formed.

[Drawing 2] It is the plan of a TFT array substrate showing a part for the connection of the shading film and the constant potential line in the gestalt of the 1st operation.

[Drawing 3] It is the cross section of the liquid crystal equipment in which the A-A' cross section of drawing 1 is shown with an opposite substrate etc.

[Drawing 4] It is the B-B' cross section of drawing 1.

[Drawing 5] It is the C-C' cross section of drawing 1.

[Drawing 6] It is the cross section of the liquid crystal equipment in which the D-D' cross section of drawing 1 is shown with an opposite substrate etc.

[Drawing 7] It is explanatory drawing having shown typically the disclination under the influence of the horizontal electric field in TN liquid crystal about various drive methods.

[Drawing 8] It is the plan of a TFT array substrate with which the liquid crystal equipment in the gestalt of operation of the 2nd of this invention is equipped and with which the data line, the scanning line, the pixel electrode, etc. were formed.
[Drawing 9] It is the B-B' cross section of drawing 8 .
[Drawing 10] It is a fragmentary sectional view in the part corresponding to the C-C' cross section of drawing 8 of the liquid crystal equipment in the gestalt of operation of the 3rd of this invention.
[Drawing 11] It is a fragmentary sectional view in the part corresponding to the B-B' cross section of drawing 8 of the liquid crystal equipment in the gestalt of operation of the 4th of this invention.
[Drawing 12] It is a fragmentary sectional view in the part corresponding to the B-B' cross section of drawing 8 of the liquid crystal equipment in the gestalt of operation of the 5th of this invention.
[Drawing 13] It is the plan showing the whole liquid crystal equipment composition in the gestalt of this operation.
[Drawing 14] It is the cross section showing the whole liquid crystal equipment composition in the gestalt of this operation.
[Drawing 15] It is a plan on the TFT array substrate which shows the two-dimensional layout of the shading film which makes shading wiring.
[Drawing 16] It is process drawing (the 1) showing order later on about the portion which showed the manufacture process of the gestalt of operation of liquid crystal equipment to drawing 4 .
[Drawing 17] It is process drawing (the 2) showing order later on about the portion which showed the manufacture process of the gestalt of operation of liquid crystal equipment to drawing 4 .
[Drawing 18] It is process drawing (the 3) showing order later on about the portion which showed the manufacture process of the gestalt of operation of liquid crystal equipment to drawing 4 .
[Drawing 19] It is process drawing (the 4) showing order later on about the portion which showed the manufacture process of the gestalt of operation of liquid crystal equipment to drawing 4 .
[Drawing 20] It is process drawing (the 1) showing order later on about the portion which showed the manufacture process of the gestalt of operation of liquid crystal equipment to drawing 6 .
[Drawing 21] It is process drawing (the 2) showing order later on about the portion which showed the manufacture process of the gestalt of operation of liquid crystal equipment to drawing 6 .
[Drawing 22] It is process drawing (the 3) showing order later on about the portion which showed the manufacture process of the gestalt of operation of liquid crystal

equipment to drawing 6 .

[Drawing 23] It is process drawing (the 4) showing order later on about the portion which showed the manufacture process of the form of operation of liquid crystal equipment to drawing 6 .

[Drawing 24] It is the block diagram showing the outline composition of the form of operation of the electronic equipment by this invention.

[Drawing 25] It is the cross section showing the liquid crystal projector as an example of electronic equipment.

[Drawing 26] It is the front view showing the personal computer as other examples of electronic equipment.

[Drawing 27] It is the decomposition perspective diagram showing the pager as an example of electronic equipment.

[Drawing 28] It is the perspective diagram showing the liquid crystal equipment using TCP as an example of electronic equipment.

[Description of Notations]

1a -- Semiconductor layer

1a' -- Field for channel formation

1b -- Low concentration source field (source side LDD field)

1c -- Low concentration drain field (drain side LDD field)

1d -- High concentration source field

1e -- High concentration drain field

1f -- The 1st storage-capacitance electrode

2 -- Insulator layer for capacity formation (gate insulator layer)

3a -- Scanning line (gate electrode)

3b -- Capacity line (the 2nd storage-capacitance electrode)

4 -- Insulator layer between the 2nd layer

5a, 5b -- Contact hole

6a -- Data line (source electrode)

6b -- Constant potential line

7 -- Insulator layer between the 3rd layer

8 -- Contact hole

9a -- Pixel electrode

10 -- TFT array substrate

11a, 11b -- Shading film (the 3rd storage-capacitance electrode)

12 -- The 1st insulator layer (lower layer of the insulator layer between the 1st layer)

12' -- Insulator layer between the 1st layer

13 -- The 2nd insulator layer (upper layer of the insulator layer between the 1st layer)

19 -- Orientation film

20 -- Opposite substrate

21 -- Counterelectrode

22 -- Orientation film

23 -- Shading layer

30 -- TFT

50 -- Liquid crystal layer

52 -- Sealant

53 -- Circumference abandonment

70 -- Storage capacitance

100 -- Liquid crystal equipment

101 -- Data-line drive circuit

104 -- Scanning-line drive circuit

CORRECTION or AMENDMENT

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[Procedure amendment 1]
[Document to be Amended] Specification.
[Item(s) to be Amended] Claim.
[Method of Amendment] Change.
[Proposed Amendment]
[Claim(s)]
[Claim 1] It comes to enclose liquid crystal between the substrates of a couple. The data line of plurality [top / substrate / of the substrate of this couple / one], Two or more scanning lines which intersect two or more of these data lines, and two or more TFT respectively connected to the data line and the scanning line of the aforementioned plurality, Two or more pixel electrodes which were respectively connected to two or more of these TFT, and have been arranged more nearly up than the aforementioned data line, Two or more 1st storage-capacitance polar zone which consisted of the same material as the semiconductor layer which constitutes the drain or source field of two or more of these TFT, and was respectively installed in the bottom of the aforementioned data line at least, It has at least one layer insulation film arranged between two or more capacity lines which contain respectively the 2nd storage-capacitance polar zone by which opposite arrangement was respectively carried out through the 1st storage-capacitance polar zone and insulator layer of the aforementioned plurality under the aforementioned data line, and aforementioned one substrate and the aforementioned pixel electrode.
The aforementioned layer insulation film is liquid crystal equipment which the field which counters the aforementioned 2nd storage-capacitance electrode section which is under the aforementioned data line at least among the aforementioned capacity lines is become depressed and formed in a concave, and is characterized

by the bird clapper.

[Claim 2] It comes to enclose liquid crystal between the substrates of a couple. The data line of plurality [top / substrate / of the substrate of this couple / one], Two or more scanning lines which intersect two or more of these data lines, and two or more TFT respectively connected to the data line and the scanning line of the aforementioned plurality, Two or more 1st storage-capacitance electrode sections which consisted of the same material as two or more pixel electrodes respectively connected to two or more of these TFT, and the semiconductor layer which constitutes the drain or source field of two or more of these TFT, and were respectively installed in the bottom of the aforementioned data line at least, Two or more capacity lines which contain respectively the 2nd storage-capacitance electrode section by which opposite arrangement was respectively carried out through the 1st storage-capacitance electrode section and the insulator layer of the aforementioned plurality under the aforementioned data line, It has the insulator layer, the insulator layer between the 2nd layer arranged between the aforementioned 2nd storage-capacitance electrode section and the aforementioned data line, and the insulator layer between the 3rd layer arranged between the aforementioned data line and the aforementioned pixel electrode between the 1st layer arranged between aforementioned one substrate and the aforementioned 1st storage-capacitance electrode section.

It is liquid crystal equipment characterized by for the field which counters the aforementioned 2nd storage-capacitance electrode section which at least one insulator layer has under the aforementioned data line at least among the aforementioned capacity lines having become depressed in the concave, and forming it among insulator layers between the above 1st, the 2nd, and the 3rd layer.

[Claim 3] Two or more aforementioned 1st storage-capacitance electrode sections are respectively installed in the scanning line of further the aforementioned plurality, and parallel.

Opposite arrangement of two or more aforementioned 2nd storage-capacitance electrode sections is further carried out through the aforementioned scanning line, the aforementioned 1st storage-capacitance electrode section installed in parallel, and the aforementioned insulator layer for capacity formation.

the above -- the liquid crystal equipment according to claim 2 characterized by becoming depressed and forming in a concave the field where one insulator layer counters the aforementioned 2nd storage-capacitance electrode section parallel to the aforementioned scanning

line among the aforementioned capacity lines further even if few

[Claim 4] The orientation film by which rubbing processing was carried out in the direction which met the aforementioned capacity line side from the aforementioned scanning-line side at the other aforementioned data line to the scanning line and the capacity line of a couple which are arranged on the aforementioned pixel electrode and put in order adjacently,

Liquid crystal equipment according to claim 3 characterized by having packed the scanning line and the capacity line of the aforementioned couple in the one band section in alignment with the aforementioned scanning line, and having a wrap shading layer further.

[Claim 5] It is liquid crystal equipment given in any 1 term of the claims 2-4 which aforementioned one substrate serves as the aforementioned insulator layer between the 1st layer, and are characterized by for the field which counters the aforementioned 2nd storage-capacitance electrode section which at least one side has under the aforementioned data line at least among the aforementioned capacity lines having become depressed in the concave, and forming it among the above 2nd and the insulator layer between the 3rd layer.

[Claim 6] Liquid crystal equipment given in any 1 term of the claims 2-5 characterized by having further the shading film prepared in the position of two or more aforementioned TFT with which the field for channel formation is seen from aforementioned one substrate side at least, and it laps respectively between the aforementioned substrate and the aforementioned insulator layer between the 1st layer.

[Claim 7] The aforementioned shading film contains the 3rd storage-capacitance electrode section prepared in at least one side and the position which counters through the aforementioned insulator layer between the 1st layer among the portion under the aforementioned data line of the aforementioned 1st storage-capacitance electrode section, and the portion parallel to the aforementioned scanning line. The aforementioned insulator layer between the 1st layer is liquid crystal equipment according to claim 6 characterized by becoming depressed and forming the field between the aforementioned 3rd storage-capacitance electrode section and the aforementioned 1st storage-capacitance electrode section in the aforementioned concave.

[Claim 8] For the aforementioned shading film, the aforementioned insulator layer between the 1st layer is liquid crystal equipment according to claim 6 or 7 characterized by being punctured while being become depressed and formed in the aforementioned concave in the position where it comes to

connect with the constant source of potential, and the aforementioned constant source of potential is connected as the aforementioned shading film.

[Claim 9] It is the manufacture method of the liquid crystal equipment characterized by including the wet etching process which forms the side attachment wall of the portion to which the aforementioned etching process became depressed in the aforementioned concave in the manufacture method of liquid crystal equipment according to claim 5 in the shape of a taper.

[Claim 10] The manufacture method of the liquid crystal equipment according to claim 6 characterized by providing the following. The process formed on the aforementioned insulator layer between the 1st layer so that the aforementioned scanning line and a capacity line may be arranged in the aforementioned pixel inter-electrode [adjoining a couple by carrying out]. The process which forms an orientation film on the portion of the aforementioned insulator layer between the 3rd layer with which the aforementioned pixel electrode top and the aforementioned pixel electrode are not formed. The process which carries out rubbing processing of this orientation film in the direction which met the aforementioned capacity line side from the aforementioned scanning-line side to the scanning line and the capacity line of the aforementioned couple at the other aforementioned data line.

[Claim 11] It is the manufacture method of liquid crystal equipment according to claim 8.

The process which forms the aforementioned shading film in the predetermined field on aforementioned one substrate,

The process which forms the aforementioned insulator layer between the 1st layer on aforementioned one substrate and a shading film so that the portion corresponding to the aforementioned position by which connection is made may become depressed in the aforementioned concave,

The process which forms the aforementioned TFT on the aforementioned insulator layer between the 1st layer,

The process which forms an insulator layer between the 2nd layer on an insulator layer between the aforementioned TFT and the 1st layer,

As a contact hole for connecting the wiring from the aforementioned constant source of potential as the aforementioned shading film As a contact hole for connecting the aforementioned TFT and the aforementioned data line between the above 2nd and the 1st layer at the same time it punctures an insulator layer until it results in the aforementioned shading film in the aforementioned position by which connection is made The process which punctures an insulator layer

between the above 2nd and the 1st layer until it results in the aforementioned semiconductor layer in the position which counters the source or the drain field of a semiconductor layer which constitutes the aforementioned TFT.

The manufacture method of the liquid crystal equipment characterized by **********.

[Claim 12] Electronic equipment characterized by equipping claims 1-11 with the liquid crystal equipment of a publication.

[Procedure amendment 2]

[Document to be Amended] Specification.

[Item(s) to be Amended] 0010.

[Method of Amendment] Change.

[Proposed Amendment]

[0010]

[Means for Solving the Problem] In order that this invention may solve the above-mentioned technical problem, it comes to enclose liquid crystal between the substrates of a couple. The data line of plurality [top / substrate / of the substrate of this couple / one], Two or more scanning lines which intersect two or more of these data lines, and two or more TFT respectively connected to the data line and the scanning line of the aforementioned plurality, Two or more pixel electrodes which were respectively connected to two or more of these TFT, and have been arranged more nearly up than the aforementioned data line, Two or more 1st storage-capacitance electrode sections which consisted of the same material as the semiconductor layer which constitutes the drain or source field of two or more of these TFT, and were respectively installed in the bottom of the aforementioned data line at least, Two or more capacity lines which contain respectively the 2nd storage-capacitance electrode section by which opposite arrangement was respectively carried out through the 1st storage-capacitance electrode section and the insulator layer of the aforementioned plurality under the aforementioned data line, It has at least one layer insulation film arranged between aforementioned one substrate and the aforementioned pixel electrode, and the field which counters the aforementioned 2nd storage-capacitance electrode section which is under the aforementioned data line at least among the aforementioned capacity lines is become depressed and formed in a concave, and the aforementioned layer insulation film is characterized by the bird clapper.

[Procedure amendment 3]

[Document to be Amended] Specification.

[Item(s) to be Amended] 0011.

[Method of Amendment] Change.

[Proposed Amendment]

[0011] According to this invention, the 1st storage-capacitance electrode section consists of the same material as the semiconductor layer which constitutes the drain or source field of TFT, and is

respectively installed in the bottom of the data line at least. Opposite arrangement of the 2nd storage-capacitance electrode section is respectively carried out through the 1st storage-capacitance electrode section and the insulator layer under the data line at least. Thus, according to this invention, since an incident light does not penetrate, the space under the data line unusable as an opening field is effectively used as a space for giving capacity to a pixel electrode.

[Procedure amendment 4]

[Document to be Amended] Specification.

[Item(s) to be Amended] 0012.

[Method of Amendment] Change.

[Proposed Amendment]

[0012] Moreover, according to this invention, the field which counters the 2nd storage-capacitance electrode section which is under the data line at least among capacity lines becomes depressed in a concave compared with other fields, and the layer insulation film is formed. Therefore, flattening of the pixel electrode side located above the data line is carried out by this hollow. For example, if only the depth equal to the 1st storage-capacitance electrode section, an insulator layer, the 2nd storage-capacitance electrode section, and the sum total thickness of the data line is hollowed to a concave, flattening of the pixel electrode side will be carried out nearly completely.

[Procedure amendment 5]

[Document to be Amended] Specification.

[Item(s) to be Amended] 0013.

[Method of Amendment] Change.

[Proposed Amendment]

[0013] As mentioned above, although it originates in the ability of rubbing processing to have not been appropriately performed with a level difference conventionally, or it originates in the deviation of the distance between substrates by the level difference directly and the poor orientation of liquid crystal tended to occur in the portion in alignment with the data line of this opening field, according to this invention, the poor orientation in this portion can be reduced by flattening.

[Procedure amendment 6]

[Document to be Amended] Specification.

[Item(s) to be Amended] 0014.

[Method of Amendment] Change.

[Proposed Amendment]

[0014] As for this invention, it comes to enclose liquid crystal between the substrates of a couple. Furthermore, the data line of plurality [top / substrate / of the substrate of this couple / one], Two or more scanning lines which intersect two or more of these data lines, and two or more TFT respectively connected to the data line and the scanning line of the aforementioned plurality, Two or more 1st storage-capacitance polar zone which consisted of the same material as two or more pixel electrodes respectively connected to two or more of these TFT,

and the semiconductor layer which constitutes the drain or source field of two or more of these TFT, and was respectively installed in the bottom of the aforementioned data line at least, Two or more capacity lines which contain respectively the 2nd storage-capacitance polar zone by which opposite arrangement was respectively carried out through the 1st storage-capacitance polar zone and insulator layer of the aforementioned plurality under the aforementioned data line, The insulator layer between the 1st layer arranged between aforementioned one substrate and the aforementioned 1st storage-capacitance polar zone, The insulator layer between the 2nd layer arranged between the aforementioned 2nd storage-capacitance polar zone and the aforementioned data line, It has the insulator layer between the 3rd layer arranged between the aforementioned data line and the aforementioned pixel electrode. among insulator layers between the above 1st, the 2nd, and the 3rd layer at least one insulator layer It is characterized by becoming depressed and forming in a concave the field which counters the aforementioned 2nd storage-capacitance polar zone which is under the aforementioned data line at least among the aforementioned capacity lines.

[Procedure amendment 7]

[Document to be Amended] Specification.

[Item(s) to be Amended] 0015.

[Method of Amendment] Change.

[Proposed Amendment]

[0015] According to this invention, the 1st storage-capacitance polar zone consists of the same material as the semiconductor layer which constitutes the drain or source field of TFT, and is respectively installed in the bottom of the data line at least. Opposite arrangement of the 2nd storage-capacitance polar zone is respectively carried out through the 1st storage-capacitance polar zone and the insulator layer under the data line at least. Thus, according to this invention, since an incident light does not penetrate, the space under the data line unusable as an opening field is effectively used as a space for giving capacity to a pixel electrode.

[Procedure amendment 8]

[Document to be Amended] Specification.

[Item(s) to be Amended] 0018.

[Method of Amendment] Change.

[Proposed Amendment]

[0018] In order that the liquid crystal equipment of this invention may solve the above-mentioned technical problem, two or more aforementioned 1st storage-capacitance polar zone further It is respectively installed in two or more aforementioned scanning lines and parallel. two or more aforementioned 2nd storage-capacitance polar zone further Opposite arrangement is carried out through the aforementioned scanning

line, the aforementioned 1st storage-capacitance polar zone installed in parallel, and the aforementioned insulator layer for capacity formation. the above -- it is characterized by becoming depressed and forming in a concave the field where one insulator layer counters the aforementioned 2nd storage-capacitance polar zone parallel to the aforementioned scanning line among the aforementioned capacity lines further even if few

[Procedure amendment 9]

[Document to be Amended] Specification.

[Item(s) to be Amended] 0019.

[Method of Amendment] Change.

[Proposed Amendment]

[0019] According to this invention, in the field where the 1st storage-capacitance polar zone and the 2nd storage-capacitance polar zone are parallel to the scanning line, opposite arrangement is carried out through the insulator layer for capacity formation. Thus, according to this invention, it is effectively used as a space for not only the bottom of the data line but a field parallel to the scanning line giving capacity to a pixel electrode. if the field where a capacity line is wired in parallel with the scanning line is generally compared with the pixel section located in an opening field here -- the [the 1st storage-capacitance polar zone, the insulator layer for capacity formation, and] -- a level difference can do only the part to which the laminating of the 2 storage-capacitance polar zone is carried out However, between the 1st, the 2nd, and the 3rd layer, among insulator layers, the field which counters the 2nd storage-capacitance polar zone parallel to the scanning line at least among capacity lines becomes depressed in a concave, and, according to this invention, at least one insulator layer is formed. Therefore, according to this hollow, flattening of the pixel electrode side formed the upper surface of an insulator layer or on this is carried out between the 3rd layer located above this capacity line. the [for example, / the 1st storage-capacitance polar zone the insulator layer for capacity formation, and] -- if only the depth equal to the sum total thickness of 2 storage-capacitance polar zone is hollowed to a concave, flattening of the pixel electrode side formed the upper surface of an insulator layer or on this between the 3rd layer will be carried out nearly completely

[Procedure amendment 10]

[Document to be Amended] Specification.

[Item(s) to be Amended] 0020.

[Method of Amendment] Change.

[Proposed Amendment]

[0020] It is characterized by for the liquid-crystal equipment of this invention to be arranged on the aforementioned pixel electrode, to have packed the orientation film by which rubbing processing was carried out in the direction which met the aforementioned

capacity line side from the aforementioned scanning-line side to the scanning line and the capacity line of a couple put in order adjacently at the other aforementioned data line, and the scanning line and the capacity line of the aforementioned couple in the one band section in alignment with the aforementioned scanning line, and to be further equipped it with a wrap shading layer.

[Procedure amendment 11]

[Document to be Amended] Specification.

[Item(s) to be Amended] 0021.

[Method of Amendment] Change.

[Proposed Amendment]

[0021] According to this invention, in the TFT array substrate, the orientation film is arranged on the pixel electrode and rubbing processing is carried out in the direction which met the capacity line side from the scanning-line side to the scanning line and the capacity line of a couple which were put in order adjacently at the other data line. Generally, to the level difference to which a field becomes high in the direction of rubbing, rubbing processing was performed comparatively good, and it has become clear that it is difficult to perform rubbing processing good to the level difference to which a field becomes low in the direction of rubbing here as a result of research by this invention person. Then, if it is made to perform rubbing processing in the direction towards the capacity line side which gave flattening like this invention from the scanning-line side which has not given flattening, since the level difference in one edge of the scanning line by the side of the pixel located in the upstream of the direction of rubbing turns into a level difference to which a field becomes high in the direction of rubbing, rubbing processing will be performed good. On the other hand, since the level difference in the edge of another side of the scanning line of the side which adjoins a capacity line turns into a level difference to which a field becomes low in the direction of rubbing, rubbing processing is not performed good. However, since it is collectively covered by the one band section of a shading layer while the field which is located above a capacity line and by which flattening was carried out is between this portion and the pixel located in the lower stream of a river of the direction of rubbing, it is distantly [from an opening field] separated. for this reason, the thing for which the poor orientation of the liquid crystal by this influences a picture even if rubbing processing is not performed good corresponding to the edge of another side of the scanning line -- most -- or there is completely nothing Temporarily, if the direction of rubbing processing is carried out reversely, you have to narrow an opening field by the level difference to which a field becomes low in the direction of rubbing appearing in the edge of the

scanning line of the one distant from a capacity line, and the poor orientation of the liquid crystal by this affecting a picture, or covering such a portion in a shading layer further.

[Procedure amendment 12]

[Document to be Amended] Specification.

[Item(s) to be Amended] 0023.

[Method of Amendment] Deletion.

[Procedure amendment 13]

[Document to be Amended] Specification.

[Item(s) to be Amended] 0024.

[Method of Amendment] Deletion.

[Procedure amendment 14]

[Document to be Amended] Specification.

[Item(s) to be Amended] 0025.

[Method of Amendment] Deletion.

[Procedure amendment 15]

[Document to be Amended] Specification.

[Item(s) to be Amended] 0026.

[Method of Amendment] Deletion.

[Procedure amendment 16]

[Document to be Amended] Specification.

[Item(s) to be Amended] 0027.

[Method of Amendment] Deletion.

[Procedure amendment 17]

[Document to be Amended] Specification.

[Item(s) to be Amended] 0028.

[Method of Amendment] Deletion.

[Procedure amendment 18]

[Document to be Amended] Specification.

[Item(s) to be Amended] 0029.

[Method of Amendment] Change.

[Proposed Amendment]

[0029] In the liquid crystal equipment of ********, aforementioned one substrate serves as the aforementioned insulator layer between the 1st layer, and at least one side is characterized by becoming depressed and forming in a concave the field which counters the aforementioned 2nd storage-capacitance polar zone which is under the aforementioned data line at least among the aforementioned capacity lines among insulator layers between the above 2nd and the 3rd layer.

[Procedure amendment 19]

[Document to be Amended] Specification.

[Item(s) to be Amended] 0030.

[Method of Amendment] Change.

[Proposed Amendment]

[0030] According to this invention, one substrate serves as the insulator layer between the 1st layer. That is, one substrate functions also as a ground film of TFT, and an insulator layer is omitted between the 1st layer. However, according to this invention, between the 2nd and the 3rd layer, among insulator layers, since the field which counters the 2nd storage-capacitance polar zone which at least one side has under the data line at least among capacity lines becomes depressed in a concave and it is formed, flattening of the upper surface of an insulator layer or a pixel electrode side is attained between the 3rd layer like an above-mentioned this invention.

[Procedure amendment 20]

[Document to be Amended] Specification.

[Item(s) to be Amended] 0031.

[Method of Amendment] Change.

[Proposed Amendment]

[0031] this invention is characterized by having further the shading film prepared in the position of two or more aforementioned TFT with which the field for channel formation is seen from aforementioned one substrate side at least, and it laps respectively between the aforementioned substrate and the aforementioned insulator layer between the 1st layer.

[Procedure amendment 21]

[Document to be Amended] Specification.

[Item(s) to be Amended] 0032.

[Method of Amendment] Change.

[Proposed Amendment]

[0032] According to this invention, the shading film is prepared in one substrate in the position of two or more TFT with which the field for channel formation is seen from one substrate side at least, and it laps respectively. Therefore, the situation in which the return light from one substrate side etc. carries out incidence to the field for channel formation concerned can be prevented, and the property of TFT does not deteriorate by generating of a photocurrent. And the shading film is prepared between one substrate and the insulator layer between the 1st layer. Therefore, while being able to carry out the electric insulation of the TFT etc. from a shading film, the situation where a shading film pollutes TFT etc. can be prevented.

[Procedure amendment 22]

[Document to be Amended] Specification.

[Item(s) to be Amended] 0033.

[Method of Amendment] Change.

[Proposed Amendment]

[0033] this invention contains the 3rd storage-capacitance polar zone by which the aforementioned shading film was prepared in the position which counters through at least one side and the aforementioned insulator layer between the 1st layer among the portion under the aforementioned data line of the aforementioned 1st storage-capacitance polar zone, and portions parallel to the aforementioned scanning line, and the aforementioned insulator layer between the 1st layer is characterized by to be become depressed and formed the field between the aforementioned 3rd storage-capacitance polar zone and the aforementioned 1st storage-capacitance polar zone in the aforementioned concave.

[Procedure amendment 23]

[Document to be Amended] Specification.

[Item(s) to be Amended] 0034.

[Method of Amendment] Change.

[Proposed Amendment]

[0034] According to this invention, the shading film contains at least one side and the 3rd storage-capacitance polar zone prepared in the position which counters through an insulator layer between the 1st layer among the portion under the data line of the 1st storage-capacitance polar zone, and the

portion parallel to the scanning line. Therefore, in addition to the capacity formed by the 1st storage-capacitance polar zone by which opposite arrangement was carried out through the insulator layer for capacity formation, and the 2nd storage-capacitance polar zone, the capacity formed by the 1st storage-capacitance polar zone by which opposite arrangement was carried out through the insulator layer between the 1st layer, and the 3rd storage-capacitance polar zone is also given to a pixel electrode as a storage capacitance. Generally the capacity formed, so that the capacity formed, so that the thickness of the insulator layer by which it is placed in between between capacity formation is thick is small and it is thin becomes large here. However, according to this invention, between the 1st layer, since the field between the 3rd storage-capacitance polar zone and the 1st storage-capacitance polar zone is become depressed and formed in the concave, an insulator layer can make thin thickness of the insulator layer by which it is placed in between between capacity formation according to the depth of a concave hollow. the [consequently, / the 1st and] -- capacity can be increased efficiently, without increasing the surface area of 3 storage-capacitance polar zone

[Procedure amendment 24]

[Document to be Amended] Specification.

[Item(s) to be Amended] 0035.

[Method of Amendment] Deletion.

[Procedure amendment 25]

[Document to be Amended] Specification.

[Item(s) to be Amended] 0036.

[Method of Amendment] Deletion.

[Procedure amendment 26]

[Document to be Amended] Specification.

[Item(s) to be Amended] 0037.

[Method of Amendment] Deletion.

[Procedure amendment 27]

[Document to be Amended] Specification.

[Item(s) to be Amended] 0038.

[Method of Amendment] Deletion.

[Procedure amendment 28]

[Document to be Amended] Specification.

[Item(s) to be Amended] 0039.

[Method of Amendment] Change.

[Proposed Amendment]

[0039] this invention is characterized by being punctured while being become depressed and formed in the aforementioned concave in the position where the aforementioned constant source of potential is connected as the aforementioned shading film by the aforementioned insulator layer between the 1st layer by coming to connect the aforementioned shading film with the constant source of potential.

[Procedure amendment 29]

[Document to be Amended] Specification.

[Item(s) to be Amended] 0040.

[Method of Amendment] Change.

[Proposed Amendment]

[0040] According to this this invention, between the 1st layer, since it is become

depressed and formed in the concave in the position where a shading film and the constant source of potential are connected, an insulator layer becomes easy [the process which punctures this position] in the manufacture process according to the depth of the portion which became depressed in this concave after insulator layer formation between the 1st layer concerned.

[Procedure amendment 30]

[Document to be Amended] Specification.

[Item(s) to be Amended] 0041.

[Method of Amendment] Deletion.

[Procedure amendment 31]

[Document to be Amended] Specification.

[Item(s) to be Amended] 0042.

[Method of Amendment] Deletion.

[Procedure amendment 32]

[Document to be Amended] Specification.

[Item(s) to be Amended] 0043.

[Method of Amendment] Deletion.

[Procedure amendment 33]

[Document to be Amended] Specification.

[Item(s) to be Amended] 0044.

[Method of Amendment] Deletion.

[Procedure amendment 34]

[Document to be Amended] Specification.

[Item(s) to be Amended] 0045.

[Method of Amendment] Change.

[Proposed Amendment]

[0045] It is the manufacture method of the liquid crystal equipment of this invention, and the aforementioned etching process is characterized by including the wet etching process which forms the side attachment wall of the portion which became depressed in the aforementioned concave at least in the shape of a taper.

[Procedure amendment 35]

[Document to be Amended] Specification.

[Item(s) to be Amended] 0046.

[Method of Amendment] Change.

[Proposed Amendment]

[0046] According to this invention, the side attachment wall of the portion which became depressed in the concave is formed in the shape of a taper of a wet etching process. Thus, if the side attachment wall of the portion which became depressed in the concave is formed in the shape of a taper, in the portion which became depressed in the concave, at a back process, it will be formed, for example, a polysilicon contest film etc. will not remain. For this reason, flattening of this portion can be carried out certainly. Moreover, it cannot be overemphasized that dry etching and wet etching may be combined.

[Procedure amendment 36]

[Document to be Amended] Specification.

[Item(s) to be Amended] 0047.

[Method of Amendment] Change.

[Proposed Amendment]

[0047] The process formed on the aforementioned insulator layer between the 1st layer so that the aforementioned scanning line and a capacity line may be arranged in the aforementioned pixel inter-electrode [adjoining a couple by

carrying out] in order that the manufacture method of the liquid crystal equipment of this invention may solve the above-mentioned technical problem, The process which forms an orientation film on the portion of the aforementioned insulator layer between the 3rd layer with which the aforementioned pixel electrode top and the aforementioned pixel electrode are not formed, It is characterized by having the process which carries out rubbing processing of this orientation film in the direction which met the aforementioned capacity line side from the aforementioned scanning-line side to the scanning line and the capacity line of the aforementioned couple at the other aforementioned data line.

[Procedure amendment 37]

[Document to be Amended] Specification.

[Item(s) to be Amended] 0048.

[Method of Amendment] Change.

[Proposed Amendment]

[0048] According to this invention, the scanning line and a capacity line are formed on an insulator layer between the 1st layer so that the scanning line and the capacity line of a couple may be located in a line with the pixel inter-electrode which adjoins each other. Next, while [the 3rd layer] the pixel electrode top and the pixel electrode are not formed, an orientation film is formed on the portion of an insulator layer. And next, rubbing processing of this orientation film is carried out in the direction which met the capacity line side from the scanning-line side to the scanning line and the capacity line of a couple at the other data line. therefore, the thing for which the poor orientation of the liquid crystal in near [this] an edge influences a picture since the edge where rubbing processing of the scanning line located in the upstream of the direction of rubbing is not performed good as mentioned above is distant from the opening field -- most -- or there is completely nothing It is very advantageous, when attaining raise in contrast, and highly minute-ization, in case a scanning-line reversal drive method is used especially as mentioned above.

[Procedure amendment 38]

[Document to be Amended] Specification.

[Item(s) to be Amended] 0049.

[Method of Amendment] Change.

[Proposed Amendment]

[0049] The process at which this invention forms the aforementioned shading film in the predetermined field on aforementioned one substrate, The process which forms the aforementioned insulator layer between the 1st layer on aforementioned one substrate and a shading film so that the portion corresponding to the aforementioned position by which connection is made may become depressed in the aforementioned concave, The process which forms Above

TFT on the aforementioned insulator layer between the 1st layer, and the process which forms an insulator layer between the 2nd layer on an insulator layer between Above TFT and the 1st layer, As a contact hole for connecting the wiring from the aforementioned constant source of potential as the aforementioned shading film As a contact hole for connecting Above TFT and the aforementioned data line between the above 2nd and the 1st layer at the same time it punctures an insulator layer until it results in the aforementioned shading film in the aforementioned position by which connection is made It is characterized by having the process which punctures the aforementioned insulator layer between the 2nd layer until it results in the aforementioned semiconductor layer in the position which counters the source or the drain field of a semiconductor layer which constitutes Above TFT.

[Procedure amendment 39]

[Document to be Amended] Specification.

[Item(s) to be Amended] 0050.

[Method of Amendment] Change.

[Proposed Amendment]

[0050] According to this invention, an insulator layer is formed between the 1st layer on a substrate and this shading film so that the portion corresponding to the position where a shading film is formed in the predetermined field on one substrate, and a shading film and the constant source of potential are connected may become depressed in a concave in while. Then, TFT is formed on an insulator layer between the 1st layer, and an insulator layer is further formed between the 2nd layer on an insulator layer between TFT and the 1st layer. Between this 2nd layer, an insulator layer is prepared in electric insulation, such as TFT, the data line, the scanning line, and a capacity line. Here, as a contact hole for connecting a shading film and the wiring from the constant source of potential, the 2nd and the insulator layer between the 1st layer are punctured, and as a contact hole for connecting TFT and the data line simultaneously until it results in a shading film, an insulator layer is punctured between the 2nd layer until it results in a semiconductor layer. Therefore, these two kinds of contact holes can be punctured collectively.

[Procedure amendment 40]

[Document to be Amended] Specification.

[Item(s) to be Amended] 0051.

[Method of Amendment] Change.

[Proposed Amendment]

[0051] this invention is characterized by equipping the above with the liquid crystal equipment of a publication.

[Procedure amendment 41]

[Document to be Amended] Specification.

[Item(s) to be Amended] 0052.

[Method of Amendment] Change.

[Proposed Amendment]

[0052] According to this invention,

electronic equipment is equipped with the liquid crystal equipment of the invention in this application mentioned above, and the high-definition image display of it becomes possible with few liquid crystal equipment with the faulty orientation of liquid crystal by the pixel electrode by which flattening was carried out.

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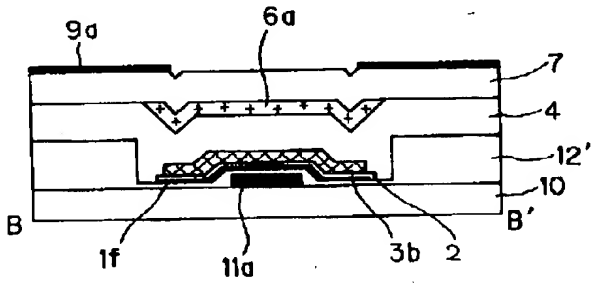
(54)【発明の名称】　液晶装置及びその製造方法並びに電子機器

(57)【要約】

【課題】　ＴＦＴ駆動によるアクティブマトリクス駆動方式の液晶装置において、画素部を平坦化しつつ画素電極の蓄積容量を増加させる。

【解決手段】　液晶装置（１００）は、一対の基板間に挟持された液晶層（５０）と、ＴＦＴアレイ基板（１０）にマトリクス状に設けられた画素電極（１１）とを備える。第１蓄積容量電極が、画素部のＴＦＴ（３０）を構成する半導体層（１ａ）からデータ線（６ａ）下に延設されている。容量線（３ｂ）は、データ線下において第１蓄積容量電極と対向配置された第２蓄積容量電極部を含む。層間絶縁膜は、このデータ線下にある蓄積容量電極に対向する領域が凹状に窪んで形成されている。



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【特許請求の範囲】

【請求項１】一対の基板間に液晶が封入されてなり、該一対の基板の一方の基板上に複数のデータ線と、該複数のデータ線に交差する複数の走査線と、前記複数のデータ線及び走査線に各々接続された複数の薄膜トランジスタと、該複数の薄膜トランジスタに各々接続されて前記データ線より上方に配置された複数の画素電極と、該複数の薄膜トランジスタのドレイン又はソース領域を構成する半導体層と同一材料からなり少なくとも前記データ線下に各々延設された複数の第１蓄積容量電極部と、前記データ線下において前記複数の第１蓄積容量電極部と絶縁膜を介して各々対向配置された第２蓄積容量電極部を各々含む複数の容量線と、前記一方の基板と前記画素電極との間に配置された少なくとも１つの層間絶縁膜とを備えており、

前記層間絶縁膜は、前記容量線のうち少なくとも前記データ線下にある前記第２蓄積容量電極部に対向する領域が凹状に窪んで形成されてなることを特徴とする液晶装置。

【請求項２】　一対の基板間に液晶が封入されてなり、該一対の基板の一方の基板上に複数のデータ線と、該複数のデータ線に交差する複数の走査線と、前記複数のデータ線及び走査線に各々接続された複数の薄膜トランジスタと、該複数の薄膜トランジスタに各々接続された複数の画素電極と、該複数の薄膜トランジスタのドレイン又はソース領域を構成する半導体層と同一材料からなり少なくとも前記データ線下に各々延設された複数の第１蓄積容量電極部と、前記データ線下において前記複数の第１蓄積容量電極部と絶縁膜を介して各々対向配置された第２蓄積容量電極部を各々含む複数の容量線と、前記一方の基板及び前記第１蓄積容量電極部の間に配置されている第１層間絶縁膜と、前記第２蓄積容量電極部及び前記データ線の間に配置されている第２層間絶縁膜と、前記データ線及び前記画素電極の間に配置されている第３層間絶縁膜とを備えており、

前記第１、第２及び第３層間絶縁膜のうち少なくとも一つの絶縁膜は、前記容量線のうち少なくとも前記データ線下にある前記第２蓄積容量電極部に対向する領域が凹状に窪んで形成されたことを特徴とする液晶装置。

【請求項３】　前記複数の第１蓄積容量電極部は更に、前記複数の走査線と平行に各々延設されており、

前記複数の第２蓄積容量電極部は更に、前記走査線と平行に延設された前記第１蓄積容量電極部と前記容量形成用絶縁膜を介して対向配置されており、

前記少なくとも一つの絶縁膜は更に、前記容量線のうち前記走査線と平行な前記第２蓄積容量電極部に対向する領域が凹状に窪んで形成されたことを特徴とする請求項２に記載の液晶装置。

【請求項４】　前記画素電極上に配置されており、隣接して並べられた一対の走査線及び容量線に対して前記走

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査線の側から前記容量線の側に向う前記データ線に沿った方向でラビング処理された配向膜と、

前記一対の走査線及び容量線を前記走査線に沿った一本の帯部でまとめて覆う遮光層とを更に備えたことを特徴とする請求項３に記載の液晶装置。

【請求項５】　前記少なくとも一つの絶縁膜は、単層から構成されていることを特徴とする請求項２から４のいずれか一項に記載の液晶装置。

【請求項６】　前記少なくとも一つの絶縁膜は、単層部分と多層部分とから構成されており、

前記単層部分が前記凹状に窪んだ部分とされており、前記多層部分が前記凹状に窪んでない部分とされていることを特徴とする請求項２から４のいずれか一項に記載の液晶装置。

【請求項７】　前記第１及び第２層間絶縁膜は、酸化シリコン膜又は窒化シリコン膜から各々構成されていることを特徴とする請求項２から６のいずれか一項に記載の液晶装置。

【請求項８】　前記第１層間絶縁膜を前記一方の基板が兼ねており、

前記第２及び第３層間絶縁膜のうち少なくとも一方は、前記容量線のうち少なくとも前記データ線下にある前記第２蓄積容量電極部に対向する領域が凹状に窪んで形成されたことを特徴とする請求項２から７のいずれか一項に記載の液晶装置。

【請求項９】　前記基板と前記第１層間絶縁膜との間において、前記複数の薄膜トランジスタの少なくともチャネル形成用領域を前記一方の基板の側から見て各々重なる位置に設けられた遮光膜を更に備えたことを特徴とする請求項２から７のいずれか一項に記載の液晶装置。

【請求項１０】　前記遮光膜は、前記第１蓄積容量電極部の前記データ線下の部分及び前記走査線と平行な部分のうち少なくとも一方と前記第１層間絶縁膜を介して対向する位置に設けられた第３蓄積容量電極部を含んでおり、

前記第１層間絶縁膜は、前記第３蓄積容量電極部と前記第１蓄積容量電極部との間の領域が前記凹状に窪んで形成されたことを特徴とする請求項９に記載の液晶装置。

【請求項１１】　前記遮光膜は、Ｔｉ、Ｃｒ、Ｗ、Ｔａ、Ｍｏ及びＰｄのうちの少なくとも一つを含むことを特徴とする請求項９又は１０に記載の液晶装置。

【請求項１２】　前記遮光膜は、定電位源に接続されていることを特徴とする請求項９から１１のいずれか一項に記載の液晶装置。

【請求項１３】　前記第１層間絶縁膜は、前記遮光膜と前記定電位源とが接続される位置において、前記凹状に窪んで形成されると共に開孔されたことを特徴とする請求項１２に記載の液晶装置。

【請求項１４】　請求項５に記載の液晶装置の製造方法であって、

前記単層を構成すべき絶縁膜を堆積する工程と、
該堆積された絶縁膜に前記凹状に窪んだ部分に対応するレジストパターンをフォトリソグラフィで形成する工程と、
該レジストパターンを介して所定時間のエッチングを行い前記凹状に窪んだ部分を形成するエッチング工程とを備えたことを特徴とする液晶装置の製造方法。

【請求項１５】　請求項６に記載の液晶装置の製造方法であって、
前記多層部分を構成すべき第１絶縁膜を堆積する工程と、
該堆積された第１絶縁膜に前記凹状に窪んだ部分に対応するレジストパターンをフォトリソグラフィで形成する工程と、
該レジストパターンを介してエッチングを行い前記凹状に窪んだ部分に対応する前記第１絶縁膜を除去するエッチング工程と、
前記単層部分及び多層部分を構成すべき第２絶縁膜を前記第１絶縁膜及び前記第１絶縁膜を除去した領域上に堆積する工程とを備えたことを特徴とする液晶装置の製造方法。

【請求項１６】　前記エッチング工程は、前記凹状に窪んだ部分の側壁をテーパ状に形成するウエットエッチング工程を含むことを特徴とする請求項１３又は１５に記載の液晶装置の製造方法。

【請求項１７】　前記走査線及び容量線を一対にして相隣接する前記画素電極間に並べるように前記第１層間絶縁膜上に形成する工程と、
前記画素電極上及び前記画素電極が形成されていない前記第３層間絶縁膜の部分上に配向膜を形成する工程と、
該配向膜を、前記一対の走査線及び容量線に対して前記走査線の側から前記容量線の側に向う前記データ線に沿った方向でラビング処理する工程とを備えたことを特徴とする請求項１４から１６のいずれか一項に記載の液晶装置の製造方法。

【請求項１８】　請求項１３に記載の液晶装置の製造方法であって、
前記一方の基板上の所定領域に前記遮光膜を形成する工程と、
前記接続される位置に対応する部分が前記凹状に窪むように前記一方の基板及び遮光膜上に前記第１層間絶縁膜を形成する工程と、
前記第１層間絶縁膜上に前記薄膜トランジスタを形成する工程と、
前記薄膜トランジスタ及び第１層間絶縁膜上に第２層間絶縁膜を形成する工程と、
前記遮光膜と前記定電位源からの配線とを接続するためのコンタクトホールとして、前記接続される位置において前記遮光膜に至るまで前記第２及び第１層間絶縁膜を開孔すると同時に、前記薄膜トランジスタと前記データ線とを接続するためのコンタクトホールとして、前記薄膜トランジスタを構成する半導体層のソース又はドレイン領域に対向する位置において前記半導体層に至るまで前記第２及び第１層間絶縁膜を開孔する工程とを備えたことを特徴とする液晶装置の製造方法。

【請求項１９】　請求項１から１３に記載の液晶装置を備えたことを特徴とする電子機器。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、薄膜トランジスタ（以下、ＴＦＴと称す）駆動によるアクティブマトリクス駆動方式の液晶装置及びその製造方法、並びにこれを用いた電子機器の技術分野に属する。

【０００２】

【従来の技術】従来、この種の液晶装置においては、一対の基板間で画素電極及び対向電極上に各々所定方向にラビング処理が施された一対の配向膜が設けられており、これらの配向膜間に液晶が所定の配向状態で挟持されている。そして、動作時には、この液晶に両電極から電界が印加され、液晶の配向状態は変化され、液晶装置の画面表示領域内で表示が行われる。

【０００３】従って、この種の液晶装置においては、データ線、走査線、容量線などの配線を形成した領域と、これらのデータ線等が形成されていない領域（特に画像表示用の入射光が通過する開口領域等）とのＴＦＴアレイ基板上の合計層厚の差による凹凸を、仮にそのまま液晶に接する面（配向膜）にまで残したとすると、その凹凸の程度に応じて液晶に配向不良（ディスクリネーション）が発生して、各画素の画像の劣化につながる。より具体的には、各開口領域が窪んだ凹凸面上に形成された配向膜に対してラビング処理を施したのでは、この凹凸に応じて配向膜表面に配向規制力のばらつきが生じ、この凹凸部で、液晶の配向不良が発生してコントラストが変化してしまう。即ち、液晶の配向不良が起こると、例えば、液晶電圧非印加時において白表示となるノーマリーホワイトモードであれば、配向不良の箇所で白抜け現象が起こり、コントラストが低下すると共に精細度も低下してしまう。このような事態を避けるべく、配向膜間の距離（液晶の層厚）を均等且つ所定値に保ち、配向膜に対するラビング処理を基板の全面に渡って均等且つ適切に施すためには、画面表示領域内に位置する画素部を平坦化することは重要である。

【０００４】他方、この種の液晶装置においては、各画素電極に画像信号を供給する際のデューティー比が小さくても、フリッカやクロストークが発生しないようにするために、各画素電極に所定容量を付与する蓄積容量を設けたりする。

【０００５】ここで、この種の液晶装置においては、画素開口率を上げて画面を明るくするという要請もあるため、このような蓄積容量を増加させるために、隣接画素

の境界として対向基板に設けられる遮光層に対応する位置にある非透明なＡｌ（アルミニウム）等からなるデータ線下やデータ線に沿った領域に、上述の如き蓄積容量が形成されたりする。より具体的には、例えば、データ線下の領域であれば、画素部におけるＴＦＴを構成する半導体層からデータ線下に延設した半導体層を第１蓄積容量電極として形成し、ゲート絶縁膜と同じ膜からなる絶縁膜をこの第１蓄積容量電極上に形成し、更に走査線と同じ層の低抵抗ポリシリコン等からなり走査線に沿って配設される容量線をその絶縁膜上に延設して、第１蓄積容量電極と絶縁膜を介して対向する第２蓄積容量電極として形成する。或いは、走査線に沿った領域であれば、画素部におけるＴＦＴを構成する半導体層から容量線下に延設した半導体層を第１蓄積容量電極として形成すると共に、ゲート絶縁膜と同じ膜からなる絶縁膜をこの第１蓄積容量電極上に形成する（この場合、第１蓄積容量電極と絶縁膜を介して対向する容量線の部分が第２蓄積容量電極として機能する）。

【０００６】このような蓄積容量を十分にとることで高精細な画像表示が可能とされる。

【０００７】

【発明が解決しようとする課題】しかしながら、前述のように蓄積容量をデータ線下の領域や走査線に沿った領域に作り込むと、この部分の層厚が増加して画素部に比較的大きな段差ができてしまう。例えば、データ線下の領域に蓄積容量を作り込むと、蓄積容量の厚み（第１蓄積容量電極、絶縁膜及び第２蓄積容量電極の合計の厚み）とデータ線の厚みだけ、これらが存在しない画素部よりも高くなることになり、その段差は約１００００ｵにもなる。このような段差があると、ラビング処理が、当該段差部分で適切に施されなくなる。この結果、データ線に沿って前述のような液晶の配向不良が起こり、コントラストや精細度が低下したりする問題点が生じる。

【０００８】逆に、このように蓄積容量を作り込んだことにより段差の増した表面を前述のように平坦化すると、製造効率やコストが悪化してしまう。特に、前述のようにデータ線下の領域に蓄積容量を形成した後に画素部の平坦化を行おうとすると、第１及び第２蓄積容量電極や容量形成用絶縁膜や該配線に付随して必要となる層間絶縁膜まで重ねたデータ線部分の合計層厚が増すため、平坦化工程に対する負担が増加して、製造効率やコストが非常に悪化してしまうという問題点がある。

【０００９】本発明は上述した問題点に鑑みなされたものであり、蓄積容量が大きく且つ画質劣化につながるような液晶の配向不良が極力低減された液晶装置及びその製造方法並びに当該液晶装置を備えた電子機器を提供することを課題とする。

【００１０】

【課題を解決するための手段】請求項１に記載の液晶装置は上記課題を解決するために、一対の基板間に液晶が

封入されてなり、該一対の基板の一方の基板上に複数のデータ線と、該複数のデータ線に交差する複数の走査線と、前記複数のデータ線及び走査線に各々接続された複数の薄膜トランジスタと、該複数の薄膜トランジスタに各々接続されて前記データ線より上方に配置された複数の画素電極と、該複数の薄膜トランジスタのドレイン又はソース領域を構成する半導体層と同一材料からなり少なくとも前記データ線下に各々延設された複数の第１蓄積容量電極部と、前記データ線下において前記複数の第１蓄積容量電極部と絶縁膜を介して各々対向配置された第２蓄積容量電極部を各々含む複数の容量線と、前記一方の基板と前記画素電極との間に配置された少なくとも１つの層間絶縁膜とを備えており、前記層間絶縁膜は、前記容量線のうち少なくとも前記データ線下にある前記第２蓄積容量電極部に対向する領域が凹状に窪んで形成されてなることを特徴とする。

【００１１】請求項１に記載の液晶装置によれば、第１蓄積容量電極部は、薄膜トランジスタのドレイン又はソース領域を構成する半導体層と同一材料からなり、少なくともデータ線下に各々延設されている。第２蓄積容量電極部は、少なくともデータ線下において第１蓄積容量電極部と絶縁膜を介して各々対向配置されている。このように本発明によれば、入射光が透過しないため開口領域としては使用不可能なデータ線下のスペースは、画素電極に対し容量を付与するためのスペースとして有効に使用されている。

【００１２】また、本発明によれば、層間絶縁膜は、容量線のうち少なくともデータ線下にある第２蓄積容量電極部に対向する領域が、他の領域と比べて凹状に窪んで形成されている。従って、データ線の上方に位置する画素電極面はこの窪みにより平坦化される。例えば、第１蓄積容量電極部、絶縁膜、第２蓄積容量電極部及びデータ線の合計層厚に等しい深さだけ凹状に窪めれば、画素電極面は、ほぼ完全に平坦化される。

【００１３】以上のように従来は、段差によりラビング処理が適切に施せなかったことに起因して、或いは段差による基板間距離の狂いに直接起因して液晶の配向不良は、この開口領域のデータ線に沿った部分で最も起き易かったが、本発明によれば、この部分における配向不良を平坦化により低減できる。

【００１４】請求項２に記載の液晶装置は上記課題を解決するために、一対の基板間に液晶が封入されてなり、該一対の基板の一方の基板上に複数のデータ線と、該複数のデータ線に交差する複数の走査線と、前記複数のデータ線及び走査線に各々接続された複数の薄膜トランジスタと、該複数の薄膜トランジスタに各々接続された複数の画素電極と、該複数の薄膜トランジスタのドレイン又はソース領域を構成する半導体層と同一材料からなり少なくとも前記データ線下に各々延設された複数の第１蓄積容量電極部と、前記データ線下において前記複数の

第１蓄積容量電極部と絶縁膜を介して各々対向配置された第２蓄積容量電極部を各々含む複数の容量線と、前記一方の基板及び前記第１蓄積容量電極部の間に配置されている第１層間絶縁膜と、前記第２蓄積容量電極部及び前記データ線の間に配置されている第２層間絶縁膜と、前記データ線及び前記画素電極の間に配置されている第３層間絶縁膜とを備えており、前記第１、第２及び第３層間絶縁膜のうち少なくとも一つの絶縁膜は、前記容量線のうち少なくとも前記データ線下にある前記第２蓄積容量電極部に対向する領域が凹状に窪んで形成されたことを特徴とする。

【００１５】請求項２に記載の液晶装置によれば、第１蓄積容量電極部は、薄膜トランジスタのドレイン又はソース領域を構成する半導体層と同一材料からなり、少なくともデータ線下に各々延設されている。第２蓄積容量電極部は、少なくともデータ線下において第１蓄積容量電極部と絶縁膜を介して各々対向配置されている。このように本発明によれば、入射光が透過しないため開口領域としては使用不可能なデータ線下のスペースは、画素電極に対し容量を付与するためのスペースとして有効に使用されている。

【００１６】他方、第１層間絶縁膜は、一方の基板及び第１蓄積容量電極部の間に配置されており、第２層間絶縁膜は、第２蓄積容量電極部及び前記データ線の間に配置されており、第３層間絶縁膜は、データ線及び画素電極の間に配置されている。ここで一般に、データ線が配線される領域は、開口領域内に位置する画素部と比較すると、半導体層と同一材料からなる第１蓄積容量電極部、絶縁膜、走査線と同じポリシリコン層等からなる容量線の第２蓄積容量電極部、Ａｌ膜等からなるデータ線が積層されている分だけ段差ができる。しかも、この段差は、液晶装置の構造上、開口領域内に位置する画素部と比較して最も大きい段差である。しかるに、本発明によれば、第１、第２及び第３層間絶縁膜のうち少なくとも一つの絶縁膜は、容量線のうち少なくともデータ線下にある第２蓄積容量電極部に対向する領域が、他の領域と比べて凹状に窪んで形成されている。従って、データ線の上方に位置する第３層間絶縁膜の上面或いはこの上に形成される画素電極面は、この窪みに応じて平坦化される。例えば、第１蓄積容量電極部、容量形成用絶縁膜、第２蓄積容量電極部及びデータ線の合計層厚に等しい深さだけ凹状に窪めれば、第３層間絶縁膜の上面或いはこの上に形成される画素電極面は、ほぼ完全に平坦化される。

【００１７】以上のように従来は、段差によりラビング処理が適切に施せなかったことに起因して、或いは段差による基板間距離の狂いに直接起因して液晶の配向不良は、この開口領域のデータ線に沿った部分で最も起き易かったが、本発明によれば、この部分における配向不良を平坦化により低減できる。

【００１８】請求項３に記載の液晶装置は上記課題を解決するために請求項２に記載の液晶装置において、前記複数の第１蓄積容量電極部は更に、前記複数の走査線と平行に各々延設されており、前記複数の第２蓄積容量電極部は更に、前記走査線と平行に延設された前記第１蓄積容量電極部と前記容量形成用絶縁膜を介して対向配置されており、前記少なくとも一つの絶縁膜は更に、前記容量線のうち前記走査線と平行な前記第２蓄積容量電極部に対向する領域が凹状に窪んで形成されたことを特徴とする。

【００１９】請求項３に記載の液晶装置によれば、第１蓄積容量電極部と第２蓄積容量電極部とは、走査線と平行な領域において、容量形成用絶縁膜を介して対向配置されている。このように本発明によれば、データ線下だけでなく、走査線に平行な領域も、画素電極に対し容量を付与するためのスペースとして有効に使用されている。ここで一般に、走査線に平行に容量線が配線される領域は、開口領域内に位置する画素部と比較すると、第１蓄積容量電極部、容量形成用絶縁膜及び第２蓄積容量電極部が積層されている分だけ段差ができる。しかるに、本発明によれば、第１、第２及び第３層間絶縁膜のうち少なくとも一つの絶縁膜は、容量線のうち少なくとも走査線と平行な第２蓄積容量電極部に対向する領域が、凹状に窪んで形成されている。従って、この容量線の上方に位置する第３層間絶縁膜の上面或いはこの上に形成される画素電極面は、この窪みに応じて平坦化される。例えば、第１蓄積容量電極部、容量形成用絶縁膜及び第２蓄積容量電極部の合計層厚に等しい深さだけ凹状に窪めれば、第３層間絶縁膜の上面或いはこの上に形成される画素電極面は、ほぼ完全に平坦化される。

【００２０】請求項４に記載の液晶装置は上記課題を解決するために請求項３に記載の液晶装置において、前記画素電極上に配置されており、隣接して並べられた一対の走査線及び容量線に対して前記走査線の側から前記容量線の側に向う前記データ線に沿った方向でラビング処理された配向膜と、前記一対の走査線及び容量線を前記走査線に沿った一本の帯部でまとめて覆う遮光層とを更に備えたことを特徴とする。

【００２１】請求項４に記載の液晶装置によれば、ＴＦＴアレイ基板において配向膜は、画素電極上に配置されており、隣接して並べられた一対の走査線及び容量線に対して走査線の側から容量線の側に向うデータ線に沿った方向でラビング処理されている。ここで一般に、ラビング方向に面が高くなる段差に対してはラビング処理は比較的良好に行われ、ラビング方向に面が低くなる段差に対してはラビング処理は良好に行うことが困難であることが本発明者による研究の結果判明している。そこで、本発明のように、平坦化を施していない走査線の側から平坦化を施した容量線の側に向けた方向でラビング処理を行うようにすれば、ラビング方向の上流に位置す

る画素側の走査線の一方の縁における段差は、ラビング方向に面が高くなる段差となるのでラビング処理が良好に行われる。他方、容量線に隣接する側の走査線の他方の縁における段差は、ラビング方向に面が低くなる段差となるのでラビング処理が良好に行われない。しかしながら、この部分とラビング方向の下流に位置する画素との間には容量線の上方に位置する平坦化された面があると共に、遮光層の一本の帯部により、まとめて覆われているので開口領域から遠く離れている。このため、走査線の他方の縁に対応してラビング処理が良好に行われなくても、これによる液晶の配向不良が画像に影響することは殆ど又は全く無い。仮に、ラビング処理の方向を反対にしてしまうと、ラビング方向に面が低くなる段差が、容量線から遠い方の走査線の縁に現われてしまい、これによる液晶の配向不良が画像に影響を及ぼしてしまうか或いは、このような部分を更に遮光層で覆うことにより開口領域を狭めねばならない。

【００２２】更に、ＴＦＴアレイ基板のラビング方向をデータ線に沿うようにした場合、直流駆動により液晶を劣化させないため及び表示画像のフリッカを防止するために走査線毎に液晶を駆動する電圧極性を反転させる走査線反転駆動方式（１Ｈ反転駆動方式）が一般化しつつあるが、この走査線反転駆動方式によれば、データ線の方向の段差である、走査線付近における画素部の段差により液晶の配向不良（ディスクリネーション）が起き易いことが、本発明者による研究の結果判明している。そこで、本発明のように、データ線の方向の段差が、一対の走査線及び容量線の縁ではなく、該一対の走査線と容量線との間にくるように構成すれば、上述の走査線反転駆動方式を採用した際に、液晶の配向不良が画素境界領域の中央付近で起きるように、即ち、各画素開口領域から離れた領域で起きるように出来る。この結果、本発明は、走査線反転駆動方式を用いる際には高コントラスト化と高精細化を図る上で、大変有利である。

【００２３】請求項５に記載の液晶装置は上記課題を解決するために請求項２から４のいずれかに記載の液晶装置において、前記少なくとも一つの絶縁膜は、単層から構成されていることを特徴とする。

【００２４】請求項５に記載の液晶装置によれば、凹状に窪んで形成される絶縁膜を単層から構成すればよいので、従来の場合と比較しても層の数を増加させる必要が無く、凹状に窪んだ部分とそうでない部分との膜厚を制御すれば、当該凹状に窪んで形成された絶縁膜が得られる。

【００２５】請求項６に記載の液晶装置は上記課題を解決するために請求項２から４に記載の液晶装置において、前記少なくとも一つの絶縁膜は、単層部分と多層部分とから構成されており、前記単層部分が前記凹状に窪んだ部分とされており、前記多層部分が前記凹状に窪んでいない部分とされていることを特徴とする。

【００２６】請求項６に記載の液晶装置によれば、単層部分が凹状に窪んだ部分とされているので、凹状に窪んだ部分における当該窪みが形成された絶縁膜の膜厚を、単層部分の膜厚として、比較的容易にして確実且つ高精度に制御できる。従って、この凹状に窪んだ部分における当該窪みが形成された絶縁膜の膜厚を非常に薄くすることも可能となる。

【００２７】請求項７に記載の液晶装置は上記課題を解決するために請求項２から６のいずれか一項に記載の液晶装置において、前記第１及び第２層間絶縁膜は、酸化シリコン膜又は窒化シリコン膜から構成されていることを特徴とする。

【００２８】請求項７に記載の液晶装置によれば、酸化シリコン膜又は窒化シリコン膜からなる第１及び第２層間絶縁膜により、一方の基板、第１蓄積容量電極部、第２蓄積容量電極部、データ線等を構成する各層を相互に電気的絶縁できると共に一方の基板等からＴＦＴへの汚染を防止できる。しかも、このように構成された第１層間絶縁膜は、ＴＦＴの下地膜に適している。

【００２９】請求項８に記載の液晶装置は上記課題を解決するために請求項２から７のいずれか一項に記載の液晶装置において、前記第１層間絶縁膜を前記一方の基板が兼ねており、前記第２及び第３層間絶縁膜のうち少なくとも一方は、前記容量線のうち少なくとも前記データ線下にある前記第２蓄積容量電極部に対向する領域が凹状に窪んで形成されたことを特徴とする。

【００３０】請求項８に記載の液晶装置によれば、一方の基板が第１層間絶縁膜を兼ねている。即ち、一方の基板がＴＦＴの下地膜としても機能し、第１層間絶縁膜は省略される。しかるに、本発明によれば、第２及び第３層間絶縁膜のうち少なくとも一方は、容量線のうち少なくともデータ線下にある第２蓄積容量電極部に対向する領域が凹状に窪んで形成されているので、上述の本発明と同様に第３層間絶縁膜の上面や画素電極面の平坦化が図られる。

【００３１】請求項９に記載の液晶装置は上記課題を解決するために請求項２から７のいずれか一項に記載の液晶装置において、前記基板と前記第１層間絶縁膜との間において、前記複数の薄膜トランジスタの少なくともチャネル形成用領域を前記一方の基板の側から見て各々重なる位置に設けられた遮光膜を更に備えたことを特徴とする。

【００３２】請求項９に記載の液晶装置によれば、遮光膜は、複数のＴＦＴの少なくともチャネル形成用領域を一方の基板の側から見て各々重なる位置において一方の基板に設けられている。従って、一方の基板の側からの戻り光等が当該チャネル形成用領域に入射する事態を未然に防ぐことができ、光電流の発生によりＴＦＴの特性が劣化することはない。そして、遮光膜は、一方の基板と第１層間絶縁膜との間に設けられている。従って、遮

光膜からＴＦＴ等を電気的絶縁し得ると共に遮光膜がＴＦＴ等を汚染する事態を未然に防げる。

【００３３】請求項１０に記載の液晶装置は上記課題を解決するために請求項９に記載の液晶装置において、前記遮光膜は、前記第１蓄積容量電極部の前記データ線下の部分及び前記走査線と平行な部分のうち少なくとも一方と前記第１層間絶縁膜を介して対向する位置に設けられた第３蓄積容量電極部を含んでおり、前記第１層間絶縁膜は、前記第３蓄積容量電極部と前記第１蓄積容量電極部との間の領域が前記凹状に窪んで形成されたことを特徴とする。

【００３４】請求項１０に記載の液晶装置によれば、遮光膜は、第１蓄積容量電極部のデータ線下の部分及び走査線と平行な部分のうち少なくとも一方と第１層間絶縁膜を介して対向する位置に設けられた第３蓄積容量電極部を含んでいる。従って、容量形成用絶縁膜を介して対向配置された第１蓄積容量電極部と第２蓄積容量電極部とで形成される容量に加えて、第１層間絶縁膜を介して対向配置された第１蓄積容量電極部と第３蓄積容量電極部とで形成される容量も、蓄積容量として画素電極に付与される。ここで一般に、容量形成用に間に介在する絶縁膜の膜厚が厚いほど形成される容量は小さく、薄いほど形成される容量は大きくなる。しかるに、本発明によれば、第１層間絶縁膜は、第３蓄積容量電極部と第１蓄積容量電極部との間の領域が凹状に窪んで形成されているため、容量形成用に間に介在する絶縁膜の膜厚を凹状の窪みの深さに応じて薄くすることが出来る。この結果、第１及び第３蓄積容量電極部の表面積を増やすことなく容量を効率的に増やすことが出来る。

【００３５】請求項１１に記載の液晶装置は上記課題を解決するために請求項９又は１０に記載の液晶装置において、前記遮光膜は、Ｔｉ（チタン）、Ｃｒ（クロム）、Ｗ（タングステン）、Ｔａ（タンタル）、Ｍｏ（モリブデン）及びＰｄ（鉛）のうちの少なくとも一つを含むことを特徴とする。

【００３６】請求項１１に記載の液晶装置によれば、遮光膜は、不透明な高融点金属であるＴｉ、Ｃｒ、Ｗ、Ｔａ、Ｍｏ及びＰｄのうちの少なくとも一つを含む、例えば、金属単体、合金、金属シリサイド等から構成されるため、ＴＦＴアレイ基板上の遮光膜形成工程の後に行われるＴＦＴ形成工程における高温処理により、遮光膜が破壊されたり溶融しないようにできる。

【００３７】請求項１２に記載の液晶装置は上記課題を解決するために請求項９から１１のいずれか一項に記載の液晶装置において、前記遮光膜は、定電位源に接続されていることを特徴とする。

【００３８】請求項１２に記載の液晶装置によれば、遮光膜は定電位源に接続されているので、遮光膜は定電位とされる。従って、遮光膜に対向配置されるＴＦＴに対し遮光膜の電位変動が悪影響を及ぼすことはない。

【００３９】請求項１３に記載の液晶装置は上記課題を解決するために請求項１２に記載の液晶装置において、前記第１層間絶縁膜は、前記遮光膜と前記定電位源とが接続される位置において、前記凹状に窪んで形成されると共に開孔されたことを特徴とする。

【００４０】請求項１３に記載の液晶装置によれば、第１層間絶縁膜は、遮光膜と定電位源とが接続される位置において凹状に窪んで形成されているので、その製造プロセスにおいて、当該第１層間絶縁膜形成後に、この凹状に窪んだ部分の深さに応じて、この位置を開孔する工程が容易となる。

【００４１】請求項１４に記載の液晶装置の製造方法は上記課題を解決するために請求項５に記載の液晶装置の製造方法であって、前記単層を構成すべき絶縁膜を堆積する工程と、該堆積された絶縁膜に前記凹状に窪んだ部分に対応するレジストパターンをフォトリソグラフィで形成する工程と、該レジストパターンを介して所定時間のエッチングを行い前記凹状に窪んだ部分を形成するエッチング工程とを備えたことを特徴とする。

【００４２】請求項１４に記載の液晶装置の製造方法によれば、先ず、一方の基板上で前記単層を構成すべき絶縁膜が、画面表示領域の全域に堆積される。次に、該堆積された絶縁膜に凹状に窪んだ部分に対応するレジストパターンが、フォトリソグラフィで形成され、その後、エッチングが、このレジストパターンを介して所定時間だけ行われて、凹状に窪んだ部分が形成される。従って、エッチングの時間管理により、凹状に窪んだ部分の深さや膜厚を制御できる。このエッチング工程において、例えばドライエッチングを用いる場合には、ほぼ露光寸法通りに開孔できる。

【００４３】請求項１５に記載の液晶装置の製造方法は上記課題を解決するために請求項６に記載の液晶装置の製造方法であって、前記多層部分を構成すべき第１絶縁膜を堆積する工程と、該堆積された第１絶縁膜に前記凹状に窪んだ部分に対応するレジストパターンをフォトリソグラフィで形成する工程と、該レジストパターンを介してエッチングを行い前記凹状に窪んだ部分に対応する前記第１絶縁膜を除去するエッチング工程と、前記単層部分及び多層部分を構成すべき第２絶縁膜を前記第１絶縁膜及び前記第１絶縁膜を除去した領域上に堆積する工程とを備えたことを特徴とする。

【００４４】請求項１５に記載の液晶装置の製造方法によれば、先ず、一方の基板上で多層部分を構成すべき第１絶縁膜が画面表示領域の全域に堆積される。次に、この堆積された第１絶縁膜に、凹状に窪んだ部分に対応するレジストパターンが、フォトリソグラフィで形成され、その後、エッチングが、このレジストパターンを介して行われて、凹状に窪んだ部分に対応する第１絶縁膜が除去される。その後、単層部分及び多層部分を構成すべき第２絶縁膜が、第１絶縁膜及び第１絶縁膜を除去し

た領域上に堆積される。この結果、凹状に窪んだ部分における第１層間絶縁膜の膜厚を、第２絶縁膜の膜厚の管理により、比較的容易にして確実且つ高精度に制御できる。このエッチング工程において、例えばドライエッチングを用いる場合には、ほぼ露光寸法通りに開孔できる。

【００４５】請求項１６に記載の液晶装置の製造方法は上記課題を解決するために請求項１４又は１５に記載の液晶装置の製造方法であって、前記エッチング工程は、少なくとも前記凹状に窪んだ部分の側壁をテーパ状に形成するウエットエッチング工程を含むことを特徴とする。

【００４６】請求項１６に記載の液晶装置の製造方法によれば、ウエットエッチング工程により、凹状に窪んだ部分の側壁は、テーパ状に形成される。このように凹状に窪んだ部分の側壁をテーパ状に形成しておけば、凹状に窪んだ部分内に後工程で形成される、例えば、ポリシリコン膜等が残ることがない。このため、この部分を確実に平坦化できる。また、ドライエッチングとウエットエッチングとを組み合わせてもよいことは言うまでもない。

【００４７】請求項１７に記載の液晶装置の製造方法は上記課題を解決するために請求項１４ら１６のいずれか一項に記載の液晶装置の製造方法であって、前記走査線及び容量線を一対にして相隣接する前記画素電極間に並べるように前記第１層間絶縁膜上に形成する工程と、前記画素電極上及び前記画素電極が形成されていない前記第３層間絶縁膜の部分上に配向膜を形成する工程と、該配向膜を、前記一対の走査線及び容量線に対して前記走査線の側から前記容量線の側に向う前記データ線に沿った方向でラビング処理する工程とを備えたことを特徴とする。

【００４８】請求項１７に記載の液晶装置の製造方法によれば、一対の走査線及び容量線は相隣接する画素電極間に並ぶように、走査線及び容量線は第１層間絶縁膜上に形成される。次に、画素電極上及び画素電極が形成されていない第３層間絶縁膜の部分上に、配向膜を形成される。そして次に、該配向膜は、一対の走査線及び容量線に対して走査線の側から容量線の側に向うデータ線に沿った方向で、ラビング処理される。従って前述のように、ラビング方向の上流に位置する走査線のラビング処理が良好に行われない縁は開口領域から離れているので、この縁付近における液晶の配向不良が画像に影響することは殆ど又は全く無い。特に前述のように走査線反転駆動方式を用いる際には高コントラスト化と高精細化を図る上で、大変有利である。

【００４９】請求項１８に記載の液晶装置の製造方法は上記課題を解決するために請求項１３に記載の液晶装置の製造方法であって、前記一方の基板上の所定領域に前記遮光膜を形成する工程と、前記接続される位置に対応

する部分が前記凹状に窪むように前記一方の基板及び遮光膜上に前記第１層間絶縁膜を形成する工程と、前記第１層間絶縁膜上に前記ＴＦＴを形成する工程と、前記ＴＦＴ及び第１層間絶縁膜上に第２層間絶縁膜を形成する工程と、前記遮光膜と前記定電位源からの配線とを接続するためのコンタクトホールとして、前記接続される位置において前記遮光膜に至るまで前記第２及び第１層間絶縁膜を開孔すると同時に、前記ＴＦＴと前記データ線とを接続するためのコンタクトホールとして、前記ＴＦＴを構成する半導体層のソース又はドレイン領域に対向する位置において前記半導体層に至るまで前記第２層間絶縁膜を開孔する工程とを備えたことを特徴とする。

【００５０】請求項１８に記載の液晶装置の製造方法によれば、一方の基板上の所定領域に遮光膜が形成され、遮光膜と定電位源とが接続される位置に対応する部分が凹状に窪むように一方の基板及びこの遮光膜上に第１層間絶縁膜が形成される。その後、ＴＦＴが第１層間絶縁膜上に形成され、更にＴＦＴ及び第１層間絶縁膜上に第２層間絶縁膜が形成される。この第２層間絶縁膜は、ＴＦＴ、データ線、走査線、容量線等の電気絶縁用に設けられるものである。ここで、遮光膜と定電位源からの配線とを接続するためのコンタクトホールとして、遮光膜に至るまで第２及び第１層間絶縁膜が開孔され、同時に、ＴＦＴとデータ線とを接続するためのコンタクトホールとして、半導体層に至るまで第２層間絶縁膜が開孔される。従って、これら２種類のコンタクトホールを一括して開孔できる。

【００５１】請求項１９に記載の電子機器は上記課題を解決するために請求項１から１３に記載の液晶装置を備えたことを特徴とする。

【００５２】請求項１９に記載の電子機器によれば、電子機器は、上述した本願発明の液晶装置を備えており、平坦化された画素電極により液晶の配向不良の少ない液晶装置により高品位の画像表示が可能となる。

【００５３】本発明のこのような作用及び他の利得は次に説明する実施の形態から明らかにする。

【００５４】

【発明の実施の形態】以下、本発明の実施の形態を図面に基づいて説明する。

【００５５】（液晶装置の第１の実施の形態）本発明による液晶装置の第１の実施の形態の構成及び動作について図１から図８に基づいて説明する。図1は、データ線、走査線、画素電極、遮光膜等が形成されたＴＦＴアレイ基板の開口領域内の画素部の平面図である。図２は、遮光膜と定電位線との接続部分の平面図である。図３は、図1のＡ－Ａ’断面を対向基板等と共に示す液晶装置の断面図である。図４は、図1のＢ－Ｂ’断面図であり、図５は、図1のＣ－Ｃ’断面図である。また図６は、図２のＤ－Ｄ’断面図である。尚、図３から図６においては、各層や各部材を図面上で認識可能な程度の大

きさとするため、各層や各部材毎に縮尺を異ならしめてある。

【００５６】図1において、液晶装置のＴＦＴアレイ基板上には、マトリクス状に複数の透明な画素電極９ａ（点線部９ａ’により輪郭が示されている）が設けられており、画素電極９ａの縦横の境界に各々沿ってデータ線６ａ（ソース電極）、走査線３ａ（ゲート電極）及び容量線３ｂが設けられている。データ線６ａは、コンタクトホール５ａを介してポリシリコン膜からなる半導体層１ａのうち後述のソース領域に電気的接続されており、画素電極９ａは、コンタクトホール８を介して半導体層１ａのうち後述のドレイン領域に電気的接続されている。また、半導体層１ａのうち後述のチャネル形成用領域１ａ’（図中右下りの斜線の領域）に対向するように走査線３ａ（ゲート電極）が配置されている。そして、図中右上がりの斜線で示した領域に画素部における遮光膜１１ａが設けられている。即ち遮光膜１１ａは、画素部において、半導体層１ａのチャネル形成用領域１ａ’を含むＴＦＴ、データ線６ａ、走査線３ａ及び容量線３ｂをＴＦＴアレイ基板の側から見て各々重なる位置に設けられている。

【００５７】図１において特に、データ線６ａ下に形成された容量線３ｂを含む太線で囲まれた領域においては、後述の第１層間絶縁膜が凹状に窪んで形成されており、それ以外の画素電極９ａ及び走査線３ａにほぼ対応する領域においては、当該第１層間絶縁膜が相対的に凸状に（平面状に）形成されている。また、ＴＦＴアレイ基板１０のラビング方向を図１の矢印の方向で行うようにすれば、本実施の形態は特に効果を発揮する。

【００５８】従って、従来は、データ線が形成される最も配向膜の形成面が高くなる段差により、ラビング処理が適切に施せなかったことに起因して、或いはこのような段差による基板間距離の狂いに直接起因して液晶の配向不良は、この開口領域のデータ線に沿った部分で最も起き易かったが、本実施の形態によれば、この部分における配向不良を平坦化により低減できる。

【００５９】図２において液晶装置のＴＦＴアレイ基板上には、データ線６ａと同じＡｌ等の導電層から形成された定電位線６ｂが設けられており、コンタクトホール５ｂを介して非画素部における遮光膜（遮光配線）１１ｂと接続されている。図２において特に、コンタクトホール５ｂを含む太線で囲まれた領域５Ｃにおいては、後述の第１層間絶縁膜が凹状に窪んで形成されており、それ以外の領域においては、当該第１層間絶縁膜が相対的に凸状に（平面状に）形成されている。

【００６０】図３から図６に示すように、液晶装置１００は、透明な一方の基板の一例を構成するＴＦＴアレイ基板１０と、これに対向配置される透明な他方の基板の一例を構成する対向基板２０とを備えている。ＴＦＴアレイ基板１０は、例えば石英基板からなり、対向基板２０は、例えばガラス基板や石英基板からなる。ＴＦＴアレイ基板１０には、画素電極９ａが設けられており、その上側には、ラビング処理等の所定の配向処理が施された配向膜１９が設けられている。画素電極９ａは例えば、ＩＴＯ膜（インジウム・ティン・オキサイド膜）などの透明導電性薄膜からなる。また配向膜１９は例えば、ポリイミド薄膜などの有機薄膜からなる。

【００６１】他方、対向基板２０には、その全面に渡って対向電極（共通電極）２１が設けられており、その下側には、ラビング処理等の所定の配向処理が施された配向膜２２が設けられている。対向電極２１は例えば、ＩＴＯ膜などの透明導電性薄膜からなる。また配向膜２２は、ポリイミド薄膜などの有機薄膜からなる。

【００６２】ＴＦＴアレイ基板１０には、図３に示すように、各画素電極９ａに隣接する位置に、各画素電極９ａをスイッチング制御する画素スイッチング用ＴＦＴ３０が設けられている。

【００６３】対向基板２０には、更に図３に示すように、各画素の開口領域以外の領域に遮光層２３が設けられている。このため、対向基板２０の側から入射光が画素スイッチング用ＴＦＴ３０の半導体層１ａのチャネル形成用領域１ａ’やＬＤＤ（Lightly Doped Drain）領域１ｂ及び１ｃに侵入することはない。更に、遮光層２３は、コントラストの向上、色材の混色防止などの機能を有する。

【００６４】このように構成され、画素電極９ａと対向電極２１とが対面するように配置されたＴＦＴアレイ基板１０と対向基板２０との間には、後述のシール材５２（図１３及び図１４参照）により囲まれた空間に液晶が封入され、液晶層５０が形成される。液晶層５０は、画素電極９ａからの電界が印加されていない状態で配向膜１９及び２２により所定の配向状態を採る。液晶層５０は、例えば一種又は数種類のネマティック液晶を混合した液晶からなる。シール材５２は、二つの基板１０及び２０をそれらの周辺で貼り合わせるための、例えば光硬化性樹脂や熱硬化性樹脂からなる接着剤であり、両基板間の距離を所定値とするためのグラスファイバー或いはガラスビーズ等のスペーサが混入されている。

【００６５】図３に示すように、画素スイッチング用ＴＦＴ３０に各々対向する位置においてＴＦＴアレイ基板１０と各画素スイッチング用ＴＦＴ３０との間には、遮光膜１１ａが各々設けられている。遮光膜１１ａは、好ましくは不透明な高融点金属であるＴｉ、Ｃｒ、Ｗ、Ｔａ、Ｍｏ及びＰｄのうちの少なくとも一つを含む、金属単体、合金、金属シリサイド等から構成される。このような材料から構成すれば、ＴＦＴアレイ基板１０上の遮光膜１１ａの形成工程の後に行われる画素スイッチング用ＴＦＴ３０の形成工程における高温処理により、遮光膜１１ａが破壊されたり溶融しないようにできる。遮光膜１１ａが形成されているので、ＴＦＴアレイ基板１０

の側からの戻り光等が画素スイッチング用ＴＦＴ３０のチャネル形成用領域１ａ’やＬＤＤ領域１ｂ、１ｃに入射する事態を未然に防ぐことができ、光電流の発生により画素スイッチング用ＴＦＴ３０の特性が劣化することはない。

【００６６】更に、遮光膜１１ａと複数の画素スイッチング用ＴＦＴ３０との間には、単層又は多層からなる第１層間絶縁膜１２’が設けられている。第１層間絶縁膜１２’は、画素スイッチング用ＴＦＴ３０を構成する半導体層１ａを遮光膜１１ａから電気的絶縁するために設けられるものである。更に、第１層間絶縁膜１２’は、ＴＦＴアレイ基板１０の全面に形成されることにより、画素スイッチング用ＴＦＴ３０のための下地膜としての機能をも有する。即ち、ＴＦＴアレイ基板１０の表面の研磨時における荒れや、洗浄後に残る汚れ等で画素スイッチング用ＴＦＴ３０の特性の劣化を防止する機能を有する。

【００６７】ここで特に図４及び図５に示すように、第１層間絶縁膜１２’は、ＴＦＴアレイ基板１０上の容量線３ｂが形成されている領域が、他の領域と比べて凹状に窪んで形成されている。後述のように、第１層間絶縁膜１２’は、単層部分と２層部分とから構成しても良いし、単層のみから構成してもよい。

【００６８】このような第１層間絶縁膜１２’は、例えば、ＮＳＧ（ノンドープトシリケートガラス）、ＰＳＧ（リンシリケートガラス）、ＢＳＧ（ボロンシリケートガラス）、ＢＰＳＧ（ボロンリンシリケートガラス）などの高絶縁性ガラス又は、酸化シリコン膜、窒化シリコン膜等からなる。

【００６９】以上の如く構成された第１層間絶縁膜１２’により、遮光膜１１ａから画素スイッチング用ＴＦＴ３０等を電気的絶縁し得ると共に遮光膜１１ａが画素スイッチング用ＴＦＴ３０等を汚染する事態を未然に防げる。ここで特に、第１層間絶縁膜１２’は、データ線６ａ下に容量線（第２蓄積容量電極）３ｂが形成された領域において凹状に窪んで形成されると共に（図４参照）、走査線３ａに沿って容量線３ｂが形成された領域において凹状に窪んで形成される（図５参照）ので、従来のように第１層間絶縁膜を平らに形成してその上に容量線３ｂを形成する場合と比較すると、凹状に窪んだ部分の深さに応じて、この容量線３ｂが形成された領域と形成されていない領域との合計層厚の差が減少し、画素部における平坦化が促進される。

【００７０】例えば、図４において、第１層間絶縁膜１２’上の遮光膜（第３蓄積容量電極）１１ａ、半導体層１ａのドレイン領域１ｅから延設された第１蓄積容量電極１ｆ、容量形成用絶縁膜（ゲート絶縁膜）２、容量線３ｂ及びデータ線６ａの合計層厚に等しくなるように凹状に窪んだ部分の深さを設定すれば、第３層間絶縁膜７の上面は、平坦となるので、その後の平坦化処理を省略できる。或いは、多少なりとも凹状に窪めれば、その後の平坦化処理の負担を軽減できる。同様に、図５において、第１層間絶縁膜１２’上の遮光膜１１ａ、半導体層１ａのドレイン領域１ｅから延設された第１蓄積容量電極１ｆ、容量形成用絶縁膜２、容量線３ｂ及びデータ線６ａの合計層厚に等しくなるように凹状に窪んだ部分の深さを設定すれば、第３層間絶縁膜７の上面は、ほぼ平坦となる（データ線６ａの分だけ画素部よりも低くなる）。但し、図４及び図５において、第１層間絶縁膜１２’は、遮光膜１１ａ、第１蓄積容量電極１ｆ、容量形成用絶縁膜２及び容量線３ｂの合計層厚に対応した深さで凹状に窪んで形成されてもよい。このように第１層間絶縁膜１２’を構成すれば、図５において、第３層間絶縁膜７の上面は、平坦となり、図４において、ほぼ平坦となる（データ線６ａの分だけ画素部よりも高くなる）。

【００７１】また、本実施の形態では特に図５に示すように、ＴＦＴアレイ基板１０上に形成された画素電極９ａ上の配向膜に対するラビング方向は、隣接して並べられた一対の走査線３ａ及び容量線３ｂに対して走査線３ａの側から容量線３ｂの側に向うデータ線６ａに沿った方向とされている。ここで一般に回転ラビング法を用いる場合、ラビング方向に面が高くなる段差に対してはラビング処理は比較的良好に行われ、ラビング方向に面が低くなる段差に対してはラビング処理は良好に行うことが困難であることが本発明者による研究の結果判明している。そこで、本実施の形態のように、平坦化を施していない走査線３ａの側から平坦化を施した容量線３ｂの側に向けた方向でラビング処理を行うようにすれば、ラビング方向の上流に位置する画素側の走査線３ａの一方の縁における段差Ｓ１は、ラビング方向に面が高くなる段差となるので配向規制力が強くラビング処理が良好に行われる。他方、容量線３ｂに隣接する側の走査線３ａの他方の縁における段差Ｓ２は、ラビング方向に面が低くなる段差となるので配向規制力が弱くラビング処理が良好に行われない。しかしながら、この段差Ｓ２とラビング方向の下流に位置する画素との間には容量線３ｂの上方に位置する平坦化された面（小さい段差Ｓ３）があると共に、遮光層２３の一本の帯部により、これら一対の走査線３ａ及び容量線３ｂは、まとめて覆われているので、段差Ｓ２は、開口領域から遠く離れている。このため、段差Ｓ２においてラビング処理が良好に行われなくても、これによる液晶の配向不良が画像に影響することは殆ど又は全く無い。仮に、ラビング処理の方向を反対にしてしまうと、ラビング方向に面が低くなる段差Ｓ１による液晶の配向不良が画像に影響を及ぼしてしまうか或いは、このような部分を更に遮光層２３で覆うことにより開口領域を狭めねばならない。従って、そのような場合は、図５において、容量線３ｂを走査線３ａに対して反対側に設けるようにすればよい。

【００７２】更に、このようにラビング処理を施すので、本実施の形態は、特にデータ線に沿ってラビングする場合には、直流駆動により液晶の劣化を生じさせないため及び表示画像のフリッカを防止するために走査線毎に液晶の両端に印加する電圧の極性を反転させる走査線反転駆動方式（１Ｈ反転駆動方式）を用いると有利である。即ち、一般に液晶の配向不良（ディスクリネーション）は、データ線の方向の段差である、走査線付近における画素部の段差により起き易い。

【００７３】ここで、このような液晶の配向不良の一例として、ＴＮ液晶における横電界の影響によるディスクリネーションを各種駆動方式について図７を参照して説明する。図７は、上から順にＤＯＴ（画素）反転駆動方式、１Ｈ（行）反転駆動方式、１Ｓ（列）反転駆動方式及び１Ｖ（フレーム）反転駆動方式について、３本の走査線及び３本のデータ線に囲まれた４つの画素開口領域におけるディスクリネーションの様子を示しており、特に左列は左回りのＴＮ液晶について右列は右回りのＴＮ液晶についてのディスクリネーションの様子を対向基板側から見た液晶装置の表示で示している。尚、図７では、横電界によりディスクリネーションが発生する領域が左下がりの斜線部で示されており、これに加えて、データ線の段差により配向不良が発生する領域が右下がりの斜線部で示されている。また、この例では、ＴＦＴアレイ基板上の配向膜に対するラビング方向が図中下から上への方向であるとする。

【００７４】図７に示すように、左回り右回りを問わずに、データ線の左右に沿った細い領域において、データ線の段差による液晶の配向不良が発生している。そして、ＤＯＴ反転駆動方式の場合には（図中、最上段参照）、左回り液晶では各走査線の上側及び各データ線の右側で横電界によるディスクリネーションが発生しており、右回り液晶では各走査線の上側及び各データ線の左側で横電界によるディスクリネーションが発生している。他方、１Ｓ反転駆動方式（液晶の両端に印加する電圧の極性をデータ線単位で反転する方式）の場合には（図中、上から３段目参照）、左回り液晶では各データ線の右側で横電界によるディスクリネーションが僅かに発生しており、右回り液晶では各データ線の左側で横電界によるディスクリネーションが僅かに発生している。そして、１Ｖ反転駆動方式（液晶の両端に印加する電圧の極性をフレームまたは垂直走査期間毎に反転する方式）の場合には（図中、最下段参照）、横電界によるディスクリネーションは走査線の上下において殆ど発生していない。

【００７５】これに対して１Ｈ反転駆動方式の場合には（図中、上から２段目参照）、右回り左回りを問わずに、各走査線の上側で横電界によるディスクリネーションが発生している。従って、図７に示したように、ＴＦＴアレイ基板上の配向膜のラビング方向を下から上の方

向にして、横電界によるディスクリネーションが発生する走査線の上側の領域に容量線を並べて設けると共に走査線の段差がこれら容量線と走査線との間に位置するように構成すれば、横電界によるディスクリネーションは、この容量線と走査線との間において主に発生することとなり、その画素開口領域に対する悪影響が低減されることになる。更に図７から、データ線部分を平坦化することにより、どの反転駆動方式においてもデータ線に沿って現われる液晶の配向不良を低減できることが分かる。

【００７６】そこで、本実施の形態では、データ線６ａの方向の段差が、一対の走査線３ａ及び容量線３ｂの縁ではなく、該一対の走査線３ａと容量線３ｂとの間にくるように構成されている。従って、走査線反転駆動方式（１Ｈ反転駆動方式）を採用した際に、液晶の配向不良が、遮光層２３で覆われた画素境界領域の中央付近で、即ち各画素開口領域から離れた領域で起きることになる。この結果、本実施の形態によれば、走査線反転駆動方式を用いた際に、電圧極性反転に伴って起きる走査線３ａに沿った液晶の配向不良が表示画像に及ぼす影響を低減でき、高コントラスト化と高精細化を図れる。

【００７７】以上のように、遮光膜１１ａを設けることにより必要となる第１層間絶縁膜１２’の所定領域が凹状に窪んで形成されているので、本実施の形態によれば、前述した従来の、平坦化膜のスピンコート等による塗布による平坦化された絶縁膜の形成等の工程を、省略又は簡略化できる。

【００７８】本実施の形態では図１及び図４に示すように、半導体層１ａの高濃度ドレイン領域１ｅは、データ線６ａに沿って延設されて第１蓄積容量電極（半導体層）１ｆとされている。従って先ず、この第１蓄積容量電極（半導体層）１ｆと容量線（第２蓄積容量電極）３ｂとの間で、容量形成用絶縁膜２を介して蓄積容量が形成される。これに加えて、遮光膜１１ａは、このデータ線６ａ下に延設された第１蓄積容量電極（半導体層）１ｆの下にも設けられているので、これら第１蓄積容量電極（半導体層）１ｆと遮光膜１１ａの間でも、第１層間絶縁膜１２’を介して容量が形成される。

【００７９】他方で、図１及び図５に示すように、半導体層１ａの高濃度ドレイン領域１ｅは、走査線３ａに平行に延設されて第１蓄積容量電極（半導体層）１ｆとされている。従って先ず、この第１蓄積容量電極（半導体層）１ｆと容量線（第２蓄積容量電極）３ｂとの間で、容量形成用絶縁膜２を介して蓄積容量が形成される。これに加えて、遮光膜１１ａは、この第１蓄積容量電極（半導体層）１ｆの下にも設けられているので、これら第１蓄積容量電極（半導体層）１ｆと遮光膜（第３蓄積容量電極）１１ａとの間で、第１層間絶縁膜１２’を介して容量が形成される。

【００８０】これらの結果、データ線６ａ下の領域及び

データ線に平行な領域という開口領域を外れたスペースを有効に利用して、画素電極９ａの蓄積容量を増やすことが出来る。

【００８１】そして本実施の形態では図１、図４及び図５に示すように、第１層間絶縁膜１２’は、これらの容量が作り込まれる領域において凹状に窪んで形成されているので平坦化が図られており、更に、この容量形成用絶縁膜としての第１層間絶縁膜１２’の凹状に窪んだ領域における層厚は非常に薄く（例えば、１０００～５０００Å程度に）構成されているので、容量線３ｂの表面積を増やすことなく、当該第１層間絶縁膜１２’を介して対向配置された遮光膜１１ａと第１蓄積容量電極１ｆとの間における容量を増やすことが出来る。このように、画素開口領域を狭めないように且つ画素部の平坦性を害さないように、蓄積容量を増加させることができるので本実施の形態は大変有利である。

【００８２】本実施の形態では図２及び図６に示すように、遮光配線部の遮光膜１１ｂ（及びこれに接続された画素部における遮光膜１１ａ）は定電位線６ｂに電気的接続されているので、遮光膜１１ａは定電位とされる。従って、遮光膜１１ａに対向配置される画素スイッチング用ＴＦＴ３０に対し遮光膜１１ａの電位変動が悪影響を及ぼすことはない。この場合、定電位線６ｂの定電位としては、接地電位に等しくてもよいし、対向電極２１の電位に等しくてもよい。また、定電位線６ｂは、液晶装置１００を駆動するための周辺回路の負電源、正電源等の定電位源に接続されてもよい。

【００８３】尚、本実施の形態では、画素スイッチング用ＴＦＴ３０に対向する領域や走査線３ａに対向する領域においては、第１層間絶縁膜１２’は凹状に窪められていない。このため、第１層間絶縁膜１２’を凹状に窪んだ領域において非常に薄くしても、凹状に窪んでいない領域における膜厚を十分な値に設定すれば、画素スイッチング用ＴＦＴ３０のチャネル形成用領域１ａ’に遮光膜１１ｂの電位が悪影響を及ぼしたり、走査線３ａと遮光膜１１ｂとの間で、寄生容量がつくような不具合はない。即ち、本実施の形態の如き構成を採れば、第１層間絶縁膜１２’の凹状に窪んだ領域における膜厚を蓄積容量増加のために、非常に薄く形成しても、画素スイッチング用ＴＦＴ３０や走査線３ａに対して悪影響を及ぼさないので、大変有利である。

【００８４】更に図２及び図６に示すように、第１層間絶縁膜１２’は、遮光膜１１ｂと定電位線６ｂとが接続される位置において、凹状に窪んで形成されているので、後述のように第１層間絶縁膜１２’形成後にコンタクトホール５ｂをエッチングにより開孔する工程が、この凹状に窪んだ部分の深さに応じて容易となり、コンタクトホール５ａと５ｂとを一括して開孔できる。従って、コンタクトホール５ｂを開孔するためだけのフォトリソグラフィ工程及びエッチング工程が削減できるため、工程数を増加させることがなく歩留まりの低下を招かない。

【００８５】再び、図３において、画素スイッチング用ＴＦＴ３０は、ＬＤＤ（Lightly Doped Drain）構造を有しており、走査線３ａ（ゲート電極）、走査線３ａからの電界によりチャネルが形成される半導体層１ａのチャネル形成用領域１ａ’、走査線３ａと半導体層１ａとを絶縁するゲート絶縁膜２、半導体層１ａの低濃度ソース領域（ソース側ＬＤＤ領域）１ｂ、データ線６ａ（ソース電極）、半導体層１ａの低濃度ドレイン領域（ドレイン側ＬＤＤ領域）１ｃ、半導体層１ａの高濃度ソース領域１ｅ及びポリシリコン層１の高濃度ドレイン領域１ｅを備えている。高濃度ドレイン領域１ｅには、複数の画素電極９ａのうちの対応する一つが接続されている。ソース領域１ｂ及び１ｄ並びにドレイン領域１ｃ及び１ｅは後述のように、半導体層１ａに対し、ｎ型又はｐ型のチャネルを形成するかに応じて所定濃度のｎ型用又はｐ型用のドーパントをドープすることにより形成されている。ｎ型チャネルのＴＦＴは、動作速度が速いという利点があり、画素のスイッチング素子である画素スイッチング用ＴＦＴ３０として用いられることが多い。本実施の形態では特にデータ線６ａ（ソース電極）は、Ａｌ等の金属膜や金属シリサイド等の合金膜などの遮光性の薄膜から構成されている。また、走査線３ａ（ゲート電極）、ゲート絶縁膜２及び第１層間絶縁膜１２’の上には、高濃度ソース領域１ｄへ通じるコンタクトホール５ａ及び高濃度ドレイン領域１ｅへ通じるコンタクトホール８が各々形成された第２層間絶縁膜４が形成されている。このソース領域１ｂへのコンタクトホール５ａを介して、データ線６ａ（ソース電極）は高濃度ソース領域１ｄに電気的接続されている。更に、データ線６ａ（ソース電極）及び第２層間絶縁膜４の上には、高濃度ドレイン領域１ｅへのコンタクトホール８が形成された第３層間絶縁膜７が形成されている。この高濃度ドレイン領域１ｅへのコンタクトホール８を介して、画素電極９ａは高濃度ドレイン領域１ｅに電気的接続されている。前述の画素電極９ａは、このように構成された第３層間絶縁膜７の上面に設けられている。

【００８６】画素スイッチング用ＴＦＴ３０は、好ましくは上述のようにＬＤＤ構造を持つが、低濃度ソース領域１ｂ及び低濃度ドレイン領域１ｃに不純物イオンの打ち込みを行わないオフセット構造を持ってよいし、ゲート電極３ａをマスクとして高濃度で不純物イオンを打ち込み、自己整合的に高濃度ソース及びドレイン領域を形成するセルフアライン型のＴＦＴであってもよい。

【００８７】また本実施の形態では、画素スイッチング用ＴＦＴ３０のゲート電極（データ線３ａ）をソース－ドレイン領域１ｂ及び１ｅ間に１個のみ配置したシングルゲート構造としたが、これらの間に２個以上のゲート電極を配置してもよい。この際、各々のゲート電極には

同一の信号が印加されるようにする。このようにデュアルゲート（ダブルゲート）以上でＴＦＴを構成すれば、チャネルとソースードレイン領域接合部のリーク電流を防止でき、オフ時の電流を低減することができる。これらのゲート電極の少なくとも１個をＬＤＤ構造或いはオフセット構造にすれば、更にオフ電流を低減でき、安定したスイッチング素子を得ることができる。

【００８８】ここで、一般には、半導体層１ａのチャネル形成用領域１ａ’、低濃度ソース領域１ｂ及び低濃度ドレイン領域１ｃ等のポリシリコン層は、光が入射するとポリシリコンが有する光電変換効果により光電流が発生してしまい画素スイッチング用ＴＦＴ３０のトランジスタ特性が劣化するが、本実施の形態では、走査線３ａ（ゲート電極）を上側から覆うようにデータ線６ａ（ソース電極）がＡｌ等の遮光性の金属薄膜から形成されているので、少なくとも半導体層１ａのチャネル形成用領域１ａ’及びＬＤＤ領域１ｂ、１ｃへの入射光（即ち、図３で上側からの光）の入射を効果的に防ぐことが出来る。また、前述のように、画素スイッチング用ＴＦＴ３０の下側には、遮光膜１１ａが設けられているので、少なくとも半導体層１ａのチャネル形成用領域１ａ’及びＬＤＤ領域１ｂ、１ｃへの戻り光（即ち、図３で下側からの光）の入射を効果的に防ぐことが出来る。

【００８９】尚、図６において、第１層間絶縁膜１２’は、２つの絶縁膜１２及び１３から構成されている。このような構成については、製造工程のところで詳述する。

【００９０】（液晶装置の第２の実施の形態）本発明による液晶装置の第２の実施の形態について図８及び図９に基づいて説明する。第２の実施の形態は、ＴＦＴアレイ基板１０側に遮光膜１１ａが設けられておらず、更に、データ線６ａ下に容量線３ｂが形成された領域でのみ、第１層間絶縁膜１２’が凹状に窪んで形成されている点で第１の実施の形態とは異なる。尚、図１に示すように遮光膜１１ａが設けられていてもよいことは言うまでもない。図８は、データ線、走査線、画素電極等が形成されたＴＦＴアレイ基板の平面図である。また図９は、図８のＢ－Ｂ’断面図である。尚、図９においては、各層や各部材を図面上で認識可能な程度の大きさとするため、各層や各部材毎に縮尺を異ならしめてある。また、第１実施の形態と同じ構成要素については同じ参照符号を付し、その説明は省略する。

【００９１】図８において、データ線６ａ下に容量線３ｂが形成された太線で囲まれた領域においては、図９に示すように第１層間絶縁膜１２’が凹状に窪んで形成されており、それ以外の容量線３ｂや画素電極９ａ及び走査線３ａにほぼ対応する領域においては、第１層間絶縁膜１２’が相対的に凸状に（平面状に）形成されている。

【００９２】従って、本実施の形態の如く平坦化処理を

何等施さなかった場合に第３層間絶縁膜７の上面で最も段差が生じる領域のみ、即ち、液晶の配向不良が最も問題になる領域のみを、第１層間絶縁膜１２’の凹状の窪みにより平坦化するので、平坦化処理にかかるコストや手間を基準にした平坦化の効率が非常に良い。

【００９３】また、図９に示した第１層間絶縁膜１２’は、第１の実施の形態の場合と同様に、単層部分と２層部分とから構成しても良く、単層のみから構成してもよい。

【００９４】本実施の形態では図９に示すように、半導体層１ａの高濃度ドレイン領域１ｅは、データ線６ａに沿って延設されて第１蓄積容量電極（半導体層）１ｆとされているので、データ線６ａに沿って延設された第１蓄積容量電極（半導体層）１ｆと容量線（第２蓄積容量電極）３ｂとの間で、第１層間絶縁膜１２’を介して容量が形成される。そして、このような容量が作り込まれる領域において平坦化が図られている。

【００９５】（液晶装置の第３の実施の形態）本発明による液晶装置の第３の実施の形態について図１０に基づいて説明する。第３の実施の形態は、ＴＦＴアレイ基板１０側に遮光膜１１ａが設けられていない点で第１の実施の形態とは異なる。図１０は、図１のＣ－Ｃ’断面に対応する位置における液晶装置の断面図である。尚、図１０においては、各層や各部材を図面上で認識可能な程度の大きさとするため、各層や各部材毎に縮尺を異ならしめてある。また、第１の実施の形態と同じ構成要素については同じ参照符号を付し、その説明は省略する。

【００９６】図１０に示すように、第３の実施の形態の液晶装置は、第１の実施の形態を示した図５と比較して、遮光膜１１ａが設けられていない。その他の構成については第１の実施の形態と同様であるので、説明を省略する。

【００９７】また、図１０に示した第１層間絶縁膜１２’は、第１の実施の形態の場合と同様に、単層部分と２層部分とから構成しても良く、単層のみから構成してもよい。

【００９８】従って、本実施の形態の如く平坦化処理を何等施さなかった場合に第３層間絶縁膜７の上面で最も段差が生じるデータ線６ａ下に容量線３ｂが形成された領域と、走査線３ａに沿って容量線３ｂが形成された領域との両方において、第１層間絶縁膜１２’の凹状の窪みにより平坦化が図られている。

【００９９】（液晶装置の第４の実施の形態）本発明による液晶装置の第４の実施の形態について図１１に基づいて説明する。第４の実施の形態は、半導体層１ａの下地膜としての第１層間絶縁膜１２’をＴＦＴアレイ基板１０が兼ねており第１層間絶縁膜１２’がなく、且つ遮光膜１１ａがない点で第１の実施の形態とは異なる。図１１は、図１のＢ－Ｂ’断面に対応する位置における液晶装置の断面図である。尚、図１１においては、各層や

各部材を図面上で認識可能な程度の大きさとするため、各層や各部材毎に縮尺を異ならしめてある。また、第１の実施の形態と同じ構成要素については同じ参照符号を付し、その説明は省略する。

【０１００】図１１に示すように、第４の実施の形態の液晶装置は、第１の実施の形態と比較して、遮光膜１１ａが設けられていない。更に、第１層間絶縁膜１２’がなく、第１蓄積容量電極（半導体層）１ｆが直接ＴＦＴアレイ基板１０の上に形成されている。そして、データ線６ａ下の容量線３ｂが形成された領域においては、第２層間絶縁膜４が凹状に窪んで形成されており、これにより、第３層間絶縁膜７の上面における平坦化が図られている。尚、走査線３ａに沿って容量線３ｂが形成された領域については、第２層間絶縁膜４を凹状に窪めて形成して平坦化してもよいし、第２の実施の形態のように平坦化しなくてもよい。

【０１０１】また、図１１に示した第２層間絶縁膜４は、第１の実施の形態における第１層間絶縁膜１２’の場合と同様に、 単層部分と２層部分とから構成しても良く、単層のみから構成してもよい。

【０１０２】このように第２層間絶縁膜４を利用して平坦化することも可能である。

【０１０３】尚、図１に示すように、遮光膜１１ａや第１層間絶縁膜１２’を設けてもよいことは言うまでもない。

【０１０４】（液晶装置の第５の実施の形態）本発明による液晶装置の第５の実施の形態について図１２に基づいて説明する。第５の実施の形態は、半導体層１ａの下地膜としての第１層間絶縁膜１２’をＴＦＴアレイ基板１０が兼ねており第１層間絶縁膜１２’がなく、且つ遮光膜１１ａがない点で第１の実施の形態とは異なる。図１２は、図１のＢ－Ｂ’断面に対応する位置における液晶装置の断面図である。尚、図１２においては、各層や各部材を図面上で認識可能な程度の大きさとするため、各層や各部材毎に縮尺を異ならしめてある。また、第１の実施の形態と同じ構成要素については同じ参照符号を付し、その説明は省略する。

【０１０５】図１２に示すように、第４の実施の形態の液晶装置は、第１の実施の形態と比較して、遮光膜１１ａが設けられていない。更に、第１層間絶縁膜１２’がなく、第１蓄積容量電極（半導体層）１ｆが直接ＴＦＴアレイ基板１０の上に形成されている。そして、データ線６ａ下の容量線３ｂが形成された領域においては、第３層間絶縁膜７が凹状に窪んで形成されており、これにより、第３層間絶縁膜７の上面における平坦化が図られている。尚、走査線３ａに沿って容量線３ｂが形成された領域については、第３層間絶縁膜７を凹状に窪めて形成して平坦化してもよいし、第２の実施の形態のように平坦化しなくてもよい。

【０１０６】また、図１２に示した第３層間絶縁膜７は、第１の実施の形態における第１層間絶縁膜１２’の場合と同様に、 単層部分と２層部分とから構成しても良く、単層のみから構成してもよい。

【０１０７】このように第３層間絶縁膜７を利用して平坦化することも可能である。

【０１０８】尚、図１に示すように、遮光膜１１ａや第１層間絶縁膜１２’を設けてもよいことは言うまでもない。

【０１０９】（液晶装置の全体構成）以上のように構成された液晶装置の各実施の形態の全体構成を図１３及び図１４を参照して説明する。尚、図１３は、ＴＦＴアレイ基板１０をその上に形成された各構成要素と共に対向基板２０の側から見た平面図であり、図１４は、対向基板２０を含めて示す図１３のＨ－Ｈ’断面図である。

【０１１０】図１３において、ＴＦＴアレイ基板１０の上には、シール材５２がその縁に沿って設けられており、その内側に並行して、例えば遮光層２３と同じ或いは異なる材料から成る遮光性の周辺見切り５３が設けられている。シール材５２の外側の領域には、データ線駆動回路１０１及び実装端子１０２がＴＦＴアレイ基板１０の一辺に沿って設けられており、走査線駆動回路１０４が、この一辺に隣接する２辺に沿って設けられている。走査線３ａに供給される走査信号遅延が問題にならないのならば、走査線駆動回路１０４は片側だけでも良いことは言うまでもない。また、データ線駆動回路１０１を画面表示領域の辺に沿って両側に配列してもよい。例えば奇数列のデータ線６ａは画面表示領域の一方の辺に沿って配設されたデータ線駆動回路から画像信号を供給し、偶数列のデータ線は前記画面表示領域の反対側の辺に沿って配設されたデータ線駆動回路から画像信号を供給するようにしてもよい。この様にデータ線６ａを櫛歯状に駆動するようにすれば、データ線駆動回路の占有面積を拡張することができるため、複雑な回路を構成することが可能となる。更にＴＦＴアレイ基板１０の残る一辺には、画面表示領域の両側に設けられた走査線駆動回路１０４間をつなぐための複数の配線１０５が設けられている。また、対向基板２０のコーナー部の少なくとも１箇所においては、ＴＦＴアレイ基板１０と対向基板２０との間で電気的導通をとるための導通材からなる銀点１０６が設けられている。そして、図１４に示すように、図１３に示したシール材５２とほぼ同じ輪郭を持つ対向基板２０が当該シール材５２によりＴＦＴアレイ基板１０に固着されている。

【０１１１】データ線駆動回路１０１及び走査線駆動回路１０４は配線によりデータ線６ａ（ソース電極）及び走査線３ａ（ゲート電極）に各々電気的接続されている。データ線駆動回路１０１には、図示しない制御回路から即時表示可能な形式に変換された画像信号が入力され、走査線駆動回路１０４がパルス的に走査線３ａに順番にゲート電圧を送るのに合わせて、データ線駆動回路

１０１は画像信号に応じた信号電圧をデータ線６ａ（ソース電極）に送る。本実施の形態では特に、画素スイッチング用ＴＦＴ３０はｐ－Ｓｉ（ポリシリコン）タイプのＴＦＴであるので、画素スイッチング用ＴＦＴ３０の形成時にほぼ同一工程で、データ線駆動回路１０１及び走査線駆動回路１０４を構成する相補型ＴＦＴを形成することも可能であり、製造上有利である。

【０１１２】次に、図１５に第１の実施の形態における遮光配線部をなす遮光膜１１ｂのＴＦＴアレイ基板１００上の２次元的レイアウトを示す。

【０１１３】図１５に示すように、遮光膜１１ａは、周辺見切り５３内の画面表示領域において走査線３ａ、容量線３ｂ及びデータ線６ａを覆うように引き回されており、画面表示領域の外側で、対向基板２０上の周辺見切り５３の下部を通るように配線し、図２に示したように定電位線に接続される。このように配線すれば、周辺見切り５３下のデッドスペースを有効に使うことが出来、シール材を硬化させる面積を広くとることが出来る。また、対向基板２０上に設けられた周辺見切り５３をＴＦＴアレイ基板１０上に遮光膜１１ａと同層で同材料で設け、遮光膜１１ａ及び１１ｂと電気的に接続するようにしてもよい。このように、周辺見切り５３を内蔵することにより対向基板２０上の遮光層は必要無くなるため、ＴＦアレイ基板１０と対向基板２０の張り合わせ時の精度は無視することが出来、透過率のばらつかない明るい液晶装置を実現できる。

【０１１４】尚、図１３から図１５において、ＴＦＴアレイ基板１０上には更に、複数のデータ線６ａに所定電圧レベルのプリチャージ信号を画像信号に先行して各々供給するプリチャージ回路、画像信号をサンプリングして複数のデータ線６ａに各々供給するサンプリング回路、製造途中や出荷時の当該液晶装置の品質、欠陥等を検査するための検査回路等を形成してもよい。また、データ線駆動回路１０１及び走査線駆動回路１０４をＴＦＴアレイ基板１０の上に設ける代わりに、例えばＴＡＢ（テープオートメイテッドボンディング基板）上に実装された駆動用ＬＳＩに、ＴＦＴアレイ基板１０の周辺部に設けられた異方性導電フィルムを介して電気的及び機械的に接続するようにしてもよい。

【０１１５】また、図１から図１５には示されていないが、対向基板２０の投射光が入射する側及びＴＦＴアレイ基板１０の出射光が出射する側には各々、例えば、ＴＮ（ツイステッドネマティック）モード、ＳＴＮ（スーパーＴＮ）モード、Ｄ－ＳＴＮ（ダブル－ＳＴＮ）モード等の動作モードや、ノーマリーホワイトモード／ノーマリーブラックモードの別に応じて、偏光フィルム、位相差フィルム、偏光板などが所定の方向で配置される。

【０１１６】次に以上のように構成された本実施の形態の動作について図３及び図１３から図１５を参照して説明する。

【０１１７】先ず、制御回路から画像信号を受けたデータ線駆動回路１０１は、この画像信号に応じたタイミング及び大きさで信号電圧をデータ線６ａ（ソース電極）に印加し、これと並行して、走査線駆動回路１０４は、所定タイミングで走査線３ａ（ゲート電極）にゲート電圧をパルス的に順次印加し、画素スイッチング用ＴＦＴ３０は駆動される。これにより、ゲート電圧がオンとされた時点でソース電圧が印加された画素スイッチング用ＴＦＴ３０においては、ソース領域１ｄ及び１ｂ、半導体層１ａのチャネル形成用領域１ａ’に形成されたチャネル並びにドレイン領域１ｃ及び１ｅを介して画素電極９ａに電圧が印加される。そして、この画素電極９ａの電圧は、ソース電圧が印加された時間よりも例えば３桁も長い時間だけ蓄積容量（図４及び図５参照）により保持される。

【０１１８】以上のように、画素電極９ａに電圧が印加されると、液晶層５０におけるこの画素電極９ａと対向電極２１とに挟まれた部分における液晶の配向状態が変化し、ノーマリーホワイトモードであれば、印加された電圧に応じて入射光がこの液晶部分を通過不可能とされ、ノーマリーブラックモードであれば、印加された電圧に応じて入射光がこの液晶部分を通過可能とされ、全体として液晶装置１００からは画像信号に応じたコントラストを持つ光が出射する。

【０１１９】特に本実施の形態では、層間絶縁膜を凹状に窪めて形成することにより画素部における平坦化が図られているため、液晶の配向不良が特に容量線が形成された領域の付近で低減されており、液晶装置１００により、高コントラストで高画質の画像を表示することが可能となる。

【０１２０】以上説明した液晶装置１００は、カラー液晶プロジェクタに適用されるため、３枚の液晶装置１００がＲＧＢ用のライトバルブとして各々用いられ、各パネルには各々ＲＧＢ色分解用のダイクロイックミラーを介して分解された各色の光が投射光として各々入射されることになる。従って、各実施の形態では、対向基板２０に、カラーフィルタは設けられていない。しかしながら、液晶装置１００においても遮光層２３の形成されていない画素電極９ａに対向する所定領域にＲＧＢのカラーフィルタをその保護膜と共に、対向基板２０上に形成してもよい。このようにすれば、液晶プロジェクタ以外の直視型や反射型のカラー液晶テレビなどのカラー液晶装置に本実施の形態の液晶装置を適用できる。更に、対向基板２０上に１画素1個対応するようにマイクロレンズを形成してもよい。このようにすれば、入射光の集光効率を向上することで、明るい液晶装置が実現できる。更にまた、対向基板２０上に、何層もの屈折率の相違する干渉層を堆積することで、光の干渉を利用して、ＲＧＢ色を作り出すダイクロイックフィルタを形成してもよ

い。このダイクロイックフィルタ付き対向基板によれば、より明るいカラー液晶装置が実現できる。

【０１２１】液晶装置１００では、従来と同様に入射光を対向基板２０の側から入射することとしたが、第１の実施の形態のように遮光膜１１ａを設けた場合には、ＴＦＴアレイ基板１０の側から入射光を入射し、対向基板２０の側から出射するようにしても良い。即ち、このように液晶装置１００を液晶プロジェクタに取り付けても、半導体層１ａのチャネル形成用領域１ａ’及びＬＤＤ領域１ｂ、１ｃに光が入射することを防ぐことが出来、高画質の画像を表示することが可能である。ここで、従来は、ＴＦＴアレイ基板１００の裏面側での反射を防止するために、反射防止用のＡＲ被膜された偏光板を別途配置したり、ＡＲフィルムを貼り付ける必要があった。しかし、第１の実施の形態では、ＴＦＴアレイ基板１０の表面と半導体層１ａの少なくともチャネル形成用領域１ａ’及びＬＤＤ領域１ｂ、１ｃとの間に遮光膜１１ａが形成されているため、このようなＡＲ被膜された偏光板やＡＲフィルムを用いたり、ＴＦＴアレイ基板１０そのものをＡＲ処理した基板を使用する必要が無くなる。従って、本実施の形態によれば、材料コストを削減でき、また偏光板貼り付け時に、ごみ、傷等により、歩留まりを落とすことがなく大変有利である。また、耐光性が優れているため、明るい光源を使用したり、偏光ビームスプリッタにより偏光変換して、光利用効率を向上させても、光によるクロストーク等の画質劣化を生じない。

【０１２２】また、液晶装置１００のスイッチング素子は、正スタガ型又はコプラナー型のポリシリコンＴＦＴであるとして説明したが、逆スタガ型のＴＦＴやアモルファスシリコンＴＦＴ等の他の形式のＴＦＴに対しても、本実施の形態は有効である。

【０１２３】更に、液晶装置１００においては、一例として液晶層５０をネマティック液晶から構成したが、液晶を高分子中に微小粒として分散させた高分子分散型液晶を用いれば、配向膜１９及び２２、並びに前述の偏光フィルム、偏光板等が不要となり、光利用効率が高まることによる液晶装置の高輝度化や低消費電力化の利点が得られる。更に、画素電極９ａをＡｌ等の反射率の高い金属膜から構成することにより、液晶装置１００を反射型液晶装置に適用する場合には、電圧無印加状態で液晶分子がほぼ垂直配向されたＳＨ（スーパーホメオトロピック）型液晶などを用いても良い。更にまた、液晶装置１００においては、液晶層５０に対し垂直な電界（縦電界）を印加するように対向基板２０の側に対向電極２１を設けているが、液晶層５０に平行な電界（横電界）を印加するように一対の横電界発生用の電極から画素電極９ａを各々構成する（即ち、対向基板２０の側には縦電界発生用の電極を設けることなく、ＴＦＴアレイ基板１０の側に横電界発生用の電極を設ける）ことも可能である。このように横電界を用いると、縦電界を用いた場合よりも視野角を広げる上で有利である。その他、各種の液晶材料（液晶相）、動作モード、液晶配列、駆動方法等に本実施の形態を適用することが可能である。

【０１２４】（製造プロセス）次に、以上のような構成を持つ液晶装置の製造プロセスについて第１の実施の形態の液晶装置を例として図１６から図２３を参照して説明する。尚、図１６から図１９は各工程におけるＴＦＴアレイ基板側の各層を、第１の実施の形態における特徴的な箇所を含む図４のＢ－Ｂ’断面に対応させて示す工程図であり、更に、図２０から図２３は各工程におけるＴＦＴアレイ基板側の各層を図６のＤ－Ｄ’断面に対応させて示す工程図である。そして、これらの図に記された工程（１）～工程（２０）は、ＴＦＴアレイ基板１上の相異なる部分における同一の工程として各々一括して行われるものである。

【０１２５】先ず、図１６から図１９を参照して、図４のＢ－Ｂ’断面に対応するデータ線３ａ並びにその下に形成された容量線３ｂ及び第１蓄積容量電極（半導体層）１ｆを含む部分の製造プロセスを中心に説明する。尚、図３のＡ－Ａ’断面に示された構成要素の製造行程や図５のＣ－Ｃ’断面に示された構成要素の製造行程も、図１６から図１９に示した各行程と一括して行われるものであるので、これらの製造工程についても各行程毎に適宜説明を加える。

【０１２６】図１６の工程（１）に示すように、石英基板、ハードガラス等のＴＦＴアレイ基板１０を用意する。ここで、好ましくはN_2（窒素）等の不活性ガス雰囲気且つ約９００～１３００℃の高温でアニール処理し、後に実施される高温プロセスにおけるＴＦＴアレイ基板１０に生じる歪みが少なくなるように前処理しておく。即ち、製造プロセスにおける最高温で高温処理される温度に合わせて、事前にＴＦＴアレイ基板１０を同じ温度かそれ以上の温度で熱処理しておく。

【０１２７】このように処理されたＴＦＴアレイ基板１０の全面に、Ｔｉ、Ｃｒ、Ｗ、Ｔａ、Ｍｏ及びＰｄ等の金属や金属シリサイド等の金属合金膜を、スパッタにより、１０００～５０００Å程度の層厚、好ましくは約２０００Åの層厚の遮光膜１１を形成する。

【０１２８】続いて、工程（２）に示すように、該形成された遮光膜１１上にフォトリソグラフィにより遮光膜１１ａのパターン（図１参照）に対応するレジストマスクを形成し、該レジストマスクを介して遮光膜１１に対しエッチングを行うことにより、遮光膜１１ａを形成する。

【０１２９】次に工程（３）に示すように、遮光膜１１ａの上に、例えば、常圧又は減圧ＣＶＤ法等によりＴＥＯＳ（テトラ・エチル・オルソ・シリケート）ガス、ＴＥＢ（テトラ・エチル・ボートレート）ガス、ＴＭＯＰ（テトラ・メチル・オキシ・フォスレート）ガス等を用

いて、ＮＳＧ、ＰＳＧ、ＢＳＧ、ＢＰＳＧなどのシリケートガラス膜、窒化シリコン膜や酸化シリコン膜等からなる第１絶縁膜１２（２層の第１層間絶縁膜１２’の下層）を形成する。この第１絶縁膜１２の層厚は、例えば、約５０００～２００００Åとし、後の工程で埋め込みたい膜の膜厚により第１絶縁膜１２の厚みを決定するようにする。

【０１３０】次に工程（４）に示すように、容量線３ｂを上方に形成する予定の領域（図１、図４及び図５参照）に対して、エッチングを行い、この領域における第１絶縁膜１２を除去する。ここで、前記エッチングを反応性エッチング、反応性イオンビームエッチング等のドライエッチングで処理した場合、フォトリソグラフィにより形成したレジストマスクとほぼ同じサイズで異方的に第１絶縁膜１２が除去できるため、設計寸法通りに容易に制御できる利点がある。一方、少なくもとウエットエッチングを用いた場合には、等方性のため、第１絶縁膜１２の開孔領域が広がるが、開孔部の側壁面をテーパー状に形成できるため、後工程の例えば走査線３ａを形成するためのポリシリコン膜３やレジストが、開孔部の側壁周囲にエッチングや剥離されずに残ってしまうことがなく、歩留まりの低下を招かない。尚、第１絶縁膜１２の開孔部の側壁面をテーパー状に形成する方法としては、ドライエッチングで一度エッチングしてから、レジストパターンを後退させて、再度ドライエッチングを行ってもよい。また、ドライエッチングとウェットエッチングを組み合わせてもよいことは言うまでもない。

【０１３１】次に工程（５）に示すように、遮光膜１１ａ及び第１絶縁膜１２の上に、第１絶縁膜１２と同様に、シリケートガラス膜、又は窒化シリコン膜や酸化シリコン膜等からなる第２絶縁膜１３（２層の第１層間絶縁膜１２’の上層）を形成する。この第２絶縁膜１３の層厚は、例えば、約１０００～２０００Åとする。第２絶縁膜１３に対し、約９００℃のアニール処理を施すことにより、汚染を防ぐと共に平坦化してもよい。

【０１３２】本実施の形態では特に、第１層間絶縁膜１２’を形成する第１絶縁膜１２及び第２絶縁膜１３の層厚は、図４に示したようにデータ線６ａ下に容量線３ｂが形成される領域において、画素電極９ａが形成される前に画素領域がほぼ平坦になるように設定される。

【０１３３】次に工程（６）に示すように、第２絶縁膜１３の上に、約４５０～５５０℃、好ましくは約５００℃の比較的低温環境中で、流量約４００～６００ｃｃ／ｍｉｎのモノシランガス、ジシランガス等を用いた減圧ＣＶＤ（例えば、圧力約２０～４０ＰａのＣＶＤ）により、アモルファスシリコン膜を形成する。その後、窒素雰囲気中で、約６００～７００℃にて約１～１０時間、好ましくは、４～６時間のアニール処理を施すことにより、ポリシリコン膜１を約５００～２０００Åの厚さ、好ましくは約１０００Åの厚さとなるまで固相成長させる。

【０１３４】この際、図３に示した画素スイッチング用ＴＦＴ３０として、ｎチャネル型の画素スイッチング用ＴＦＴ３０を作成する場合には、当該チャネル形成用領域にＳｂ（アンチモン）、Ａｓ（砒素）、Ｐ（リン）などのＶ族元素のドーパントを僅かにイオン注入等によりドープする。また、画素スイッチング用ＴＦＴ３０をｐチャネル型とする場合には、Ｂ（ボロン）、Ｇａ（ガリウム）、Ｉｎ（インジウム）などのIII族元素のドーパントを僅かにイオン注入等によりドープする。尚、アモルファスシリコン膜を経ないで、減圧ＣＶＤ法等によりポリシリコン膜１を直接形成しても良い。或いは、減圧ＣＶＤ法等により堆積したポリシリコン膜にシリコンイオンを打ち込んで一旦非晶質化（アモルファス化）し、その後アニール処理等により再結晶化させてポリシリコン膜１を形成しても良い。

【０１３５】次に図１７の工程（７）に示すように、フォトリソグラフィ工程、エッチング工程等により、図１に示した如き所定パターンの半導体層１ａを形成する。即ち、特にデータ線６ａ下で容量線３ｂが形成される領域及び走査線３ａに沿って容量線３ｂが形成される領域には、画素スイッチング用ＴＦＴ３０を構成する半導体層１ａ（図３参照）から延設された第１蓄積容量電極（半導体層）１ｆを形成する（図４及び図５参照）。

【０１３６】次に工程（８）に示すように、画素スイッチング用ＴＦＴ３０を構成する半導体層１ａと共に第１蓄積容量電極（半導体層）１ｆを約９００～１３００℃の温度、好ましくは約１０００℃の温度により熱酸化することにより、約３００Åの比較的薄い厚さの熱酸化シリコン膜を形成し、更に減圧ＣＶＤ法等により高温酸化シリコン膜（ＨＴＯ膜）や窒化シリコン膜を約５００Åの比較的薄い厚さに堆積し、多層構造を持つ画素スイッチング用ＴＦＴ３０のゲート絶縁膜２（図３参照）と共に容量形成用絶縁膜２を形成する（図４及び図５参照）。この結果、第１蓄積容量電極１ｆ（半導体層１ａ）の厚さは、約３００～１５００Åの厚さ、好ましくは約３５０～５００Åの厚さとなり、容量形成用絶縁膜（ゲート絶縁膜）２の厚さは、約２００～１５００Åの厚さ、好ましくは約３００～１０００Åの厚さとなる。このように高温熱酸化時間を短くすることにより、特に８インチ程度の大型ウエーハを使用する場合に熱によるそりを防止することができる。但し、ポリシリコン層１を熱酸化することのみにより、単一層構造を持つ容量形成用絶縁膜２（ゲート絶縁膜２）を形成してもよい。

【０１３７】尚、工程（８）において特に限定されないが、第１蓄積容量電極１ｆとなる半導体層部分に、例えば、Ｐイオンをドーズ量約3×10^{12}／cm^2でドープして、低抵抗化させてもよい。

【０１３８】次に工程（９）に示すように、減圧ＣＶＤ法等によりポリシリコン層３を堆積した後、リン（Ｐ）

を熱拡散し、ポリシリコン膜３を導電化する。又は、Ｐイオンをポリシリコン膜３の成膜と同時に導入したドープトシリコン膜を用いてもよい。工程（１０）に示すように、レジストマスクを用いたフォトリソグラフィ工程、エッチング工程等により、図１に示した如き所定パターンの走査線３ａ（ゲート電極）と共に容量線３ｂを形成する。これらの容量線３ｂ（走査線３ａ）の層厚は、例えば、約３５００Åとされる。

【０１３９】但し、容量線３ｂや走査線３ａを、ポリシリコン層ではなく、ＷやＭｏ等の高融点金属膜又は金属シリサイド膜から形成してもよいし、若しくはこれらの金属膜又は金属シリサイド膜とポリシリコン膜を組み合わせて多層に形成してもよい。この場合、容量線３ｂや走査線３ａを、遮光層２３が覆う領域の一部又は全部に対応する遮光膜として配置すれば、金属膜や金属シリサイド膜の持つ遮光性により、遮光層２３の一部或いは全部を省略することも可能となる。この場合特に、対向基板２０とＴＦＴアレイ基板１０との貼り合わせずれによる画素開口率の低下を防ぐことが出来る利点がある。

【０１４０】次に工程（１１）に示すように、図３に示した画素スイッチング用ＴＦＴ３０をＬＤＤ構造を持つｎチャネル型のＴＦＴとする場合、半導体層１ａに、先ず低濃度ソース領域１ｂ及び低濃度ドレイン領域１ｃを形成するために、走査線３ａ（ゲート電極）を拡散マスクとして、Ｐなどの５族元素のドーパント２００を低濃度で（例えば、Ｐイオンを$1\sim3\times10^{13}$／cm^2のドーズ量にて）ドープする。これにより走査線３ａ（ゲート電極）下の半導体層１ａはチャネル形成用領域１ａ’となる。この不純物のドープにより容量線３ｂ及び走査線３ａも低抵抗化される（図４及び図５参照）。

【０１４１】続いて、図１８の工程（１２）に示すように、画素スイッチング用ＴＦＴ３０を構成する高濃度ソース領域１ｂ及び高濃度ドレイン領域１ｃを形成するために、走査線３ａ（ゲート電極）よりも幅の広いマスクでレジスト層２０２を走査線３ａ（ゲート電極）上に形成した後、同じくＰなどの５族元素のドーパント２０１を高濃度で（例えば、Ｐイオンを$1\sim3\times10^{15}$／cm^2のドーズ量にて）ドープする。また、画素スイッチング用ＴＦＴ３０をｐチャネル型とする場合、半導体層１ａに、低濃度ソース領域１ｂ及び低濃度ドレイン領域１ｃ並びに高濃度ソース領域１ｄ及び高濃度ドレイン領域１ｅを形成するために、Ｂなどの３族元素のドーパントを用いてドープする。このようにＬＤＤ構造とした場合、ショートチャネル効果を低減できる利点が得られる。尚、例えば、低濃度のドープを行わずに、オフセット構造のＴＦＴとしてもよく、走査線３ａ（ゲート電極）をマスクとして、Ｐイオン、Ｂイオン等を用いたイオン注入技術によりセルフアライン型のＴＦＴとしてもよい。

【０１４２】この不純物のドープにより容量線３ｂ及び走査線３ａも更に低抵抗化される（図４及び図５参照）。

【０１４３】これらの工程と並行して、ｎチャネル型ＴＦＴ及びｐチャネル型ＴＦＴから構成される相補型構造を持つデータ線駆動回路１０１及び走査線駆動回路１０４をＴＦＴアレイ基板１０上の周辺部に形成する。このように、本実施の形態において画素スイッチング用ＴＦＴ３０はポリシリコンＴＦＴであるので、画素スイッチング用ＴＦＴ３０の形成時にほぼ同一工程で、データ線駆動回路１０１及び走査線駆動回路１０４を形成することができ、製造上有利である。

【０１４４】次に工程（１３）に示すように、画素スイッチング用ＴＦＴ３０における走査線３ａ（ゲート電極）と共に容量線３ｂ及び走査線３ａを覆うように（図４及び図５参照）、例えば、常圧又は減圧ＣＶＤ法やＴＥＯＳガス等を用いて、ＮＳＧ、ＰＳＧ、ＢＳＧ、ＢＰＳＧなどのシリケートガラス膜、窒化シリコン膜や酸化シリコン膜等からなる第２層間絶縁膜４を形成する。第２層間絶縁膜４の層厚は、約５０００～１５０００Åが好ましい。

【０１４５】次に工程（１４）の段階で、図３に示すように高濃度ソース領域１ｄ及び高濃度ドレイン領域１ｅを活性化するために約１０００℃のアニール処理を２０分程度行った後、データ線３１（ソース電極）に対するコンタクトホール５ａを、反応性エッチング、反応性イオンビームエッチング等のドライエッチングにより形成する。この際、反応性エッチング、反応性イオンビームエッチングのような異方性エッチングにより、コンタクトホール５ａ等を開孔した方が、開孔形状をマスク形状とほぼ同じにできるという利点がある。但し、ドライエッチングとウエットエッチングとを組み合わせて開孔すれば、これらのコンタクトホール５ａ等をテーパ状にできるので、配線接続時の断線を防止できるという利点が得られる。また、走査線３ａや容量線３ｂ（図５参照）を図示しない配線と接続するためのコンタクトホールも、コンタクトホール５ａと同一の工程により第２層間絶縁膜４に開孔する。

【０１４６】次に工程（１５）に示すように、第２層間絶縁膜４の上に、スパッタ処理等により、遮光性のＡｌ等の低抵抗金属や金属シリサイド等を金属膜６として、約１０００～５０００Åの厚さ、好ましくは約３０００Åに堆積し、更に工程（１６）に示すように、フォトリソグラフィ工程、エッチング工程等により、データ線６ａ（ソース電極）を形成する。

【０１４７】次に図１９の工程（１７）に示すように、データ線６ａ（ソース電極）上を覆うように、例えば、常圧又は減圧ＣＶＤ法やＴＥＯＳガス等を用いて、ＮＳＧ、ＰＳＧ、ＢＳＧ、ＢＰＳＧなどのシリケートガラス膜、窒化シリコン膜や酸化シリコン膜等からなる第３層間絶縁膜７を形成する。第３層間絶縁膜７の層厚は、約

５０００～１５０００Åが好ましい。

【０１４８】本実施の形態では、特に図１６の工程（４）及び（５）により、容量線３ｂが形成される領域において、第１層間絶縁膜が凹状に窪んで形成されているため、この工程（１７）を終えた段階で、容量線３ｂの上方に位置する画素領域の表面はほぼ平坦となる。尚、液晶装置１００において、ＴＦＴアレイ基板１０側における液晶分子の配向不良を更に抑制するために、第３層間絶縁膜７の上に更に平坦化膜をスピンコート等で塗布してもよく、又はＣＭＰ処理を施してもよい。或いは、第３層間絶縁膜７を平坦化膜で形成してもよい。本実施の形態では、図４から図６等に示したように、第１層間絶縁膜１２’の凹状の窪みにより容量線等が形成された部分とそれ以外の部分とが殆ど同じ高さとされるため、このような平坦化処理は一般に必要でないが、より高品位の画像を表示するために、このように最上層部において更なる平坦化を行う場合にも、平坦化膜を非常に薄くできたり、平坦化処理を僅かに加えるだけです済むので本実施の形態は、大変有利である。

【０１４９】次に工程（１８）の段階において、図３に示すように、画素スイッチング用ＴＦＴ３０において、画素電極９ａと高濃度ドレイン領域１ｅとを電気的接続するためのコンタクトホール８を、反応性エッチング、反応性イオンビームエッチング等のドライエッチングにより形成する。この際、反応性エッチング、反応性イオンビームエッチングのような異方性エッチングにより、コンタクトホール８を開孔した方が、開孔形状をマスク形状とほぼ同じにできるという利点が得られる。但し、ドライエッチングとウエットエッチングとを組み合わせて開孔すれば、コンタクトホール８をテーパ状にできるので、配線接続時の断線を防止できるという利点が得られる。

【０１５０】次に工程（１９）に示すように、第３層間絶縁膜７の上に、スパッタ処理等により、ＩＴＯ膜等の透明導電性薄膜９を、約５００～２０００Åの厚さに堆積し、更に工程（２０）に示すように、フォトリソグラフィ工程、エッチング工程等により、画素電極９ａを形成する。尚、当該液晶装置１００を反射型の液晶装置に用いる場合には、Ａｌ等の反射率の高い不透明な材料から画素電極９ａを形成してもよい。

【０１５１】続いて、画素電極９ａの上にポリイミド系の配向膜の塗布液を塗布した後、所定のプレティルト角を持つように且つ所定方向でラビング処理を施すこと等により、図３に示した配向膜１９が形成される。

【０１５２】他方、図３に示した対向基板２０については、ガラス基板等が先ず用意され、遮光層２３及び遮光性の周辺見切り５３が、例えば金属クロムをスパッタした後、フォトリソグラフィ工程、エッチング工程を経て形成される。尚、遮光層２３及び周辺見切り５３は、Ｃｒ、Ｎｉ、Ａｌなどの金属材料の他、カーボンやＴｉをフォトレジストに分散した樹脂ブラックなどの材料から形成してもよい。

【０１５３】その後、対向基板２０の全面にスパッタ処理等により、ＩＴＯ等の透明導電性薄膜を、約５００～２０００Åの厚さに堆積することにより、対向電極２１を形成する。更に、対向電極２１の全面にポリイミド系の配向膜の塗布液を塗布した後、所定のプレティルト角を持つように且つ所定方向でラビング処理を施すこと等により、配向膜２２が形成される。

【０１５４】本実施の形態では、前述のように、データ線６ａに沿って相隣接した走査線３ａの側から容量線３ｂの側に向かう方向でラビング処理が行われる。これにより、その性質上ラビング処理が困難な段差Ｓ２（図５参照）が遮光層２３により覆われる境界領域の中央付近に位置するため、この段差Ｓ２における配向不良が画素開口領域に悪影響を及ぼすことが殆ど又は全くない。

【０１５５】最後に、上述のように各層が形成されたＴＦＴアレイ基板１０と対向基板２０とは、配向膜１９及び２２が対面するようにシール材５２により貼り合わされ、真空吸引等により、両基板間の空間に、例えば複数種類のネマティック液晶を混合してなる液晶が吸引されて、所定層厚の液晶層５０が形成される。

【０１５６】次に、図２０から図２３を参照して、図６のＤ－Ｄ’断面に対応する遮光膜と定電位線との接続部分を含む部分の製造プロセスについて説明する。

【０１５７】図２０の工程（１）から図２３の工程（２０）は、前述した図１６の工程（１）から図１９の工程（２０）と同一の製造プロセスとして行われる。

【０１５８】即ち、図２０の工程（１）に示すように、ＴＦＴアレイ基板１０の全面に遮光膜１１を形成した後、工程（２）に示すように、フォトリソグラフィ工程、エッチング工程等により遮光膜１１ｂを形成する。

【０１５９】次に工程（３）に示すように、遮光膜１１ｂの上に、第１絶縁膜１２（２層の第１層間絶縁膜１２’の下層）を形成し、工程（４）に示すように、接続部分を上方に形成する予定の領域に対して、エッチングを行い、この領域における第１絶縁膜１２を除去する。ここで、エッチングを反応性エッチング、反応性イオンビームエッチング等のドライエッチングで処理した場合、フォトリソグラフィにより形成したレジストマスクとほぼ同じサイズで異方的に第１絶縁膜１２が除去できるため、設計寸法通りに容易に制御できる利点がある。一方、少なくともウエットエッチングを用いた場合には、等方性のため、第１絶縁膜１２の開孔領域が広がるが、開孔部の側壁面をテーパー状に形成できるため、後工程の例えば走査線３ａを形成するためのポリシリコン膜やレジストが、開孔部の側壁周囲にエッチングや剥離されずに残ってしまうことがなく、歩留まりの低下を招かない。尚、第１絶縁膜１２の開孔部の側壁面をテーパー状に形成する方法としては、ドライエッチングで一度

エッチングしてから、レジストパターンを後退させて、再度ドライエッチングを行ってもよい。

【０１６０】その後、工程（５）に示すように、遮光膜１１ｂ及び第１絶縁膜１２の上に、第２絶縁膜１３（２層の第１層間絶縁膜１２’の上層）を形成する。

【０１６１】次に工程（６）に示すように、第２絶縁膜１３上にアモルファスシリコン膜を形成した後、ポリシリコン膜１を固相成長させる。

【０１６２】次に図２１の工程（７）及び（８）では、画素部における半導体層１ａとゲート絶縁膜２の形成を待ち、その後、工程（９）に示すように、ポリシリコン層３を一旦堆積した後、工程（１０）に示すように、この接続部分ではポリシリコン層３は全て除去される。

【０１６３】次に図２１の工程（１１）及び図２２の工程（１２）に示すように、半導体層１ａのための不純物イオンのドープが終了する。

【０１６４】次に工程（１３）に示すように、第１絶縁膜１３を覆うように、第２層間絶縁膜４を形成し、工程（１４）に示すように、遮光膜１１ｂと定電位線６ｂとを接続するためのコンタクトホール５ｂを第２層間絶縁膜４に開ける。この際、第２層間絶縁膜４の下に形成されているのは第１層間絶縁膜１２’のうち第２絶縁膜１３だけなので、半導体層１ａの高濃度ソース領域１ｄ上で第２層間絶縁膜４を開孔して、コンタクトホール５ａを形成する工程（図１８の工程（１４））と同じエッチング工程で一気に開孔できる。

【０１６５】次に工程（１５）に示すように、第２層間絶縁膜４の上に、スパッタ処理等により、Ａｌ等を金属膜６として堆積した後に、工程（１６）に示すように、フォトリソグラフィ工程、エッチング工程等により、データ線と同一層（Ａｌ等）からなる定電位線６ｂを形成する。

【０１６６】次に図２３の工程（１７）に示すように、定電位線６ｂ及び第２層間絶縁膜４上を覆うように、第３層間絶縁膜７を形成する。

【０１６７】次に工程（１８）では、図３に示すコンタクトホール８が開孔されるのを待った後、工程（１９）に示すように、第３層間絶縁膜７の上に、ＩＴＯ膜等の透明導電性薄膜９を一旦堆積し、更に工程（２０）に示すように、フォトリソグラフィ工程、エッチング工程等によりこの部分については全て除去する。

【０１６８】以上のように本実施の形態における液晶装置の製造方法によれば、遮光膜１１ｂと定電位線６ｂとを接続するためのコンタクトホール５ｂとして、遮光膜１１ｂに至るまで第２層間絶縁膜４及び第１絶縁膜１３（第１層間絶縁膜の上層）が開孔され、同時に、画素スイッチング用ＴＦＴ３０とデータ線６ａとを接続するためのコンタクトホール５ａとして、半導体層１ａに至るまで第２層間絶縁膜４が開孔される。従って、これら２種類のコンタクトホール５ａ及び５ｂを一括して開孔できるので、製造上有利である。例えば、選択比を適当な値に設定してのウエットエッチングにより、このような２種類のコンタクトホール５ａ及び５ｂを各々所定の深さとなるように一括して開孔することが可能となる。特に、第１層間絶縁膜の凹状に窪んだ部分の深さに応じて、これらのコンタクトホールを開孔する工程が容易となる。遮光膜と定電位線を接続するためのコンタクトホール開孔工程（フォトリソグラフィ工程、エッチング工程等）が削除できるので、工程増による製造コストの増大や歩留まりの低下を招かない。

【０１６９】以上説明したように本実施の形態における製造プロセスによれば、凹状に窪んだ部分における第１層間絶縁膜１２’の層厚を、第２絶縁膜１３の層厚の管理により、比較的容易にして確実且つ高精度に制御できる。従って、この凹状に窪んだ部分における第１層間絶縁膜１２’の層厚を非常に薄くすることも可能となる。

【０１７０】尚、第１層間絶縁膜１２を単層から構成する場合には、図１６及び図２０に各々示した工程（３）、（４）及び（５）に若干の変更を加えて、工程（１）から（２０）を行えばよい。即ち、工程（３）において、遮光膜１１ａの上に、例えば、約１００００～１５０００Åといったように若干厚めの単層の第１層間絶縁膜１２を堆積し、工程（４）において、容量線３ｂを上方に形成する予定の領域に対して、エッチングを行い、この領域における第１層間絶縁膜１２を１０００～２０００Å程度の厚みを残すようにする。そして、工程（５）を省略する。この場合にも、第１層間絶縁膜１２のエッチングしない部分の層厚とエッチングした部分の層厚とは、後に画素電極９ａが形成される前に画素領域がほぼ平坦になるように設定される。このように第１層間絶縁膜１２を単層から構成すれば、従来の場合と比較しても層の数を増加させる必要が無く、凹状に窪んだ部分とそうでない部分との層厚をエッチング時間管理により制御すれば平坦化を図れるので便利である。

【０１７１】（電子機器）次に、以上詳細に説明した液晶装置１００を備えた電子機器の実施の形態について図２４から図２８を参照して説明する。

【０１７２】先ず図２４に、このように液晶装置１００を備えた電子機器の概略構成を示す。

【０１７３】図２４において、電子機器は、表示情報出力源１０００、表示情報処理回路１００２、駆動回路１００４、液晶装置１００、クロック発生回路１００８並びに電源回路１０１０を備えて構成されている。表示情報出力源１０００は、ＲＯＭ（Read Only Memory）、ＲＡＭ（Random Access Memory）、光ディスク装置などのメモリ、画像信号を同調して出力する同調回路等を含み、クロック発生回路１００８からのクロック信号に基づいて、所定フォーマットの画像信号などの表示情報を表示情報処理回路１００２に出力する。表示情報処理回路１００２は、増幅・極性反転回路、相展開回路、ロー

テーション回路、ガンマ補正回路、クランプ回路等の周知の各種処理回路を含んで構成されており、クロック信号に基づいて入力された表示情報からデジタル信号を順次生成し、クロック信号CLKと共に駆動回路１００４に出力する。駆動回路１００４は、液晶装置１００を駆動する。電源回路１０１０は、上述の各回路に所定電源を供給する。尚、液晶装置１００を構成するＴＦＴアレイ基板の上に、駆動回路１００４を搭載してもよく、これに加えて表示情報処理回路１００２を搭載してもよい。

【０１７４】次に図２５から図２８に、このように構成された電子機器の具体例を各々示す。

【０１７５】図２５において、電子機器の一例たる液晶プロジェクタ１１００は、上述した駆動回路１００４がＴＦＴアレイ基板上に搭載された液晶装置１００を含む液晶モジュールを３個用意し、各々ＲＧＢ用のライトバルブ１００Ｒ、１００Ｇ及び１００Ｂとして用いたプロジェクタとして構成されている。液晶プロジェクタ１１００では、メタルハライドランプ等の白色光源のランプユニット１１０２から投射光が発せられると、３枚のミラー１１０６及び２枚のダイクロイックミラー１１０８によって、ＲＧＢの３原色に対応する光成分Ｒ、Ｇ、Ｂに分けられ、各色に対応するライトバルブ１００Ｒ、１００Ｇ及び１００Ｂに各々導かれる。この際特にＢ光は、長い光路による光損失を防ぐために、入射レンズ１１２２、リレーレンズ１１２３及び出射レンズ１１２４からなるリレーレンズ系１１２１を介して導かれる。そして、ライトバルブ１００Ｒ、１００Ｇ及び１００Ｂにより各々変調された３原色に対応する光成分は、ダイクロイックプリズム１１１２により再度合成された後、投射レンズ１１１４を介してスクリーン１１２０にカラー画像として投射される。

【０１７６】本実施の形態では特に、遮光膜がＴＦＴの下側にも設けられているため、当該液晶装置１００からの投射光に基づく液晶プロジェクタ内の投射光学系による反射光、投射光が通過する際のＴＦＴアレイ基板の表面からの反射光、他の液晶装置から出射した後にダイクロイックプリズム１１１２を突き抜けてくる投射光の一部等が、戻り光としてＴＦＴアレイ基板の側から入射しても、画素電極のスイッチング用のＴＦＴ等のチャネル領域に対する遮光を十分に行うことができる。このため、小型化に適したプリズムを投射光学系に用いても、各液晶装置のＴＦＴアレイ基板とプリズムとの間において、戻り光防止用のＡＲフィルムを貼り付けたり、偏光板にＡＲ被膜処理を施したりすることが不要となるので、構成を小型且つ簡易化する上で大変有利である。

【０１７７】図２６において、電子機器の他の例たるマルチメディア対応のラップトップ型のパーソナルコンピュータ（ＰＣ）１２００は、上述した液晶装置１００がトップカバーケース内に備えられており、更にＣＰＵ、メモリ、モデム等を収容すると共にキーボード１２０２が組み込まれた本体１２０４を備えている。

【０１７８】図２７において、電子機器の他の例たるページャ１３００は、金属フレーム１３０２内に前述の駆動回路１００４がＴＦＴアレイ基板上に搭載されて液晶表示モジュールをなす液晶装置１００が、バックライト１３０６ａを含むライトガイド１３０６、回路基板１３０８、第１及び第２のシールド板１３１０及び１３１２、二つの弾性導電体１３１４及び１３１６、並びにフィルムキャリアテープ１３１８と共に収容されている。この例の場合、前述の表示情報処理回路１００２（図２４参照）は、回路基板１３０８に搭載してもよく、液晶装置１００のＴＦＴアレイ基板上に搭載してもよい。更に、前述の駆動回路１００４を回路基板１３０８上に搭載することも可能である。

【０１７９】尚、図２７に示す例はページャであるので、回路基板１３０８等が設けられている。しかしながら、駆動回路１００４や更に表示情報処理回路１００２を搭載して液晶モジュールをなす液晶装置１００の場合には、金属フレーム１３０２内に液晶装置１００を固定したものを液晶装置として、或いはこれに加えてライトガイド１３０６を組み込んだバックライト式の液晶装置として、生産、販売、使用等することも可能である。

【０１８０】また図２８に示すように、駆動回路１００４や表示情報処理回路１００２を搭載しない液晶装置１００の場合には、駆動回路１００４や表示情報処理回路１００２を含むＩＣ１３２４がポリイミドテープ１３２２上に実装されたＴＣＰ（Tape Carrier Package）１３２０に、ＴＦＴアレイ基板１０の周辺部に設けられた異方性導電フィルムを介して物理的且つ電気的に接続して、液晶装置として、生産、販売、使用等することも可能である。

【０１８１】以上図２５から図２８を参照して説明した電子機器の他にも、液晶テレビ、ビューファインダ型又はモニタ直視型のビデオテープレコーダ、カーナビゲーション装置、電子手帳、電卓、ワードプロセッサ、エンジニアリング・ワークステーション（ＥＷＳ）、携帯電話、テレビ電話、ＰＯＳ端末、タッチパネルを備えた装置等などが図２４に示した電子機器の例として挙げられる。

【０１８２】以上説明したように、本実施の形態によれば、製造効率が高く、高コントラストで高品位の画像表示が可能な液晶装置１００を備えた各種の電子機器を実現できる。

【０１８３】

【発明の効果】本発明の液晶装置によれば、画素開口領域として使用不可能なデータ線下のスペースや走査線に沿った画素境界のスペースを、画素電極に対し蓄積容量を付与するために有効利用できると同時に、データ線の上方に位置する画素部付近の平坦化が図られており、この付近で最も起き易かった液晶の配向不良を効率的に低

減でき、高コントラストで高精細な画像表示が可能となる。他方、所定方向でラビング処理を施すことにより、ラビング処理を適切に施すことが困難で液晶の配向不良が起き易い箇所を画像表示に悪影響を及ぼさない位置に配置でき、言い換えれば画素開口率を効率的に高めることも可能となる。特に、走査線反転駆動方式（１Ｈ反転駆動方式）を使用した際に、この効果は顕著に現われる。また、平坦化のために凹状に窪められ、従って薄い絶縁膜部分を容量形成用絶縁膜として利用することで、画素電極の蓄積容量を限られたスペースの中で効率的に増加できる。更に、ＴＦＴの下側に配置した遮光膜をも利用して、この蓄積容量を更に効率的に増加できる。更にまた、遮光膜と定電位源との接続を容易にすることも可能である。

【０１８４】他方、本発明の液晶装置の製造方法によれば、比較的簡単な工程制御により或いは信頼性の高い工程により、本発明の液晶装置を製造するが可能となる。また、容量形成用絶縁膜を非常に薄くすることにより、画素電極の蓄積容量を効率的に増加することも可能となる。更に、各種のコンタクトホールを一括して開孔することにより、液晶装置における低コスト化を図ることも可能である。

【０１８５】また、本発明の電子機器によれば、液晶の配向不良による画質の低下が低減されており、高コントラストで高品位の画像表示が可能であり、しかも低コストの液晶プロジェクタ、パーソナルコンピュータ、ページャ等の様々な電子機器を実現可能となる。

【図面の簡単な説明】

【図１】　本発明の第１の実施の形態における液晶装置に備えられる、データ線、走査線、画素電極、遮光膜等が形成されたＴＦＴアレイ基板の平面図である。

【図２】　第１の実施の形態における遮光膜と定電位線との接続部分を示すＴＦＴアレイ基板の平面図である。

【図３】　図1のＡ－Ａ’断面を対向基板等と共に示す液晶装置の断面図である。

【図４】　図1のＢ－Ｂ’断面図である。

【図５】　図1のＣ－Ｃ’断面図である。

【図６】　図1のＤ－Ｄ’断面を対向基板等と共に示す液晶装置の断面図である。

【図７】　ＴＮ液晶における横電界の影響によるディスクリネーションを各種駆動方式について模式的に示した説明図である。

【図８】　本発明の第２の実施の形態における液晶装置に備えられる、データ線、走査線、画素電極等が形成されたＴＦＴアレイ基板の平面図である。

【図９】　図８のＢ－Ｂ’断面図である。

【図１０】　本発明の第３の実施の形態における液晶装置の図８のＣ－Ｃ’断面に対応する箇所における部分断面図である。

【図１１】　本発明の第４の実施の形態における液晶装置の図８のＢ－Ｂ’断面に対応する箇所における部分断面図である。

【図１２】　本発明の第５の実施の形態における液晶装置の図８のＢ－Ｂ’断面に対応する箇所における部分断面図である。

【図１３】　本実施の形態における液晶装置の全体構成を示す平面図である。

【図１４】　本実施の形態における液晶装置の全体構成を示す断面図である。

【図１５】　遮光配線をなす遮光膜の２次元的レイアウトを示すＴＦＴアレイ基板上の平面図である。

【図１６】　液晶装置の実施の形態の製造プロセスを図４に示した部分について順を追って示す工程図（その１）である。

【図１７】　液晶装置の実施の形態の製造プロセスを図４に示した部分について順を追って示す工程図（その２）である。

【図１８】　液晶装置の実施の形態の製造プロセスを図４に示した部分について順を追って示す工程図（その３）である。

【図１９】　液晶装置の実施の形態の製造プロセスを図４に示した部分について順を追って示す工程図（その４）である。

【図２０】　液晶装置の実施の形態の製造プロセスを図６に示した部分について順を追って示す工程図（その１）である。

【図２１】　液晶装置の実施の形態の製造プロセスを図６に示した部分について順を追って示す工程図（その２）である。

【図２２】　液晶装置の実施の形態の製造プロセスを図６に示した部分について順を追って示す工程図（その３）である。

【図２３】　液晶装置の実施の形態の製造プロセスを図６に示した部分について順を追って示す工程図（その４）である。

【図２４】　本発明による電子機器の実施の形態の概略構成を示すブロック図である。

【図２５】　電子機器の一例としての液晶プロジェクタを示す断面図である。

【図２６】　電子機器の他の例としてのパーソナルコンピュータを示す正面図である。

【図２７】　電子機器の一例としてのページャを示す分解斜視図である。

【図２８】　電子機器の一例としてのＴＣＰを用いた液晶装置を示す斜視図である。

【符号の説明】

１ａ…半導体層

１ａ’…チャネル形成用領域

１ｂ…低濃度ソース領域（ソース側ＬＤＤ領域）

１ｃ…低濃度ドレイン領域（ドレイン側ＬＤＤ領域）

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１ｄ…高濃度ソース領域
１ｅ…高濃度ドレイン領域
１ｆ…第１蓄積容量電極
２…容量形成用絶縁膜（ゲート絶縁膜）
３ａ…走査線（ゲート電極）
３ｂ…容量線（第２蓄積容量電極）
４…第２層間絶縁膜
５ａ、５ｂ…コンタクトホール
６ａ…データ線（ソース電極）
６ｂ…定電位線
７…第３層間絶縁膜
８…コンタクトホール
９ａ…画素電極
１０…ＴＦＴアレイ基板
１１ａ、１１ｂ…遮光膜（第３蓄積容量電極）
１２…第１絶縁膜（第１層間絶縁膜の下層）

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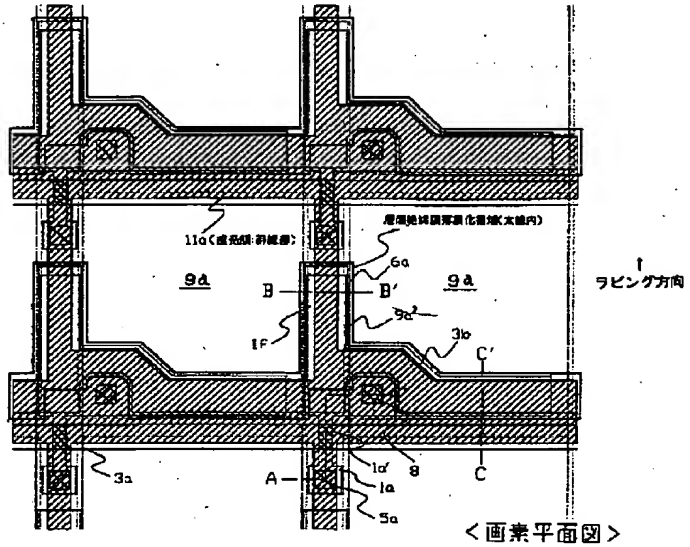
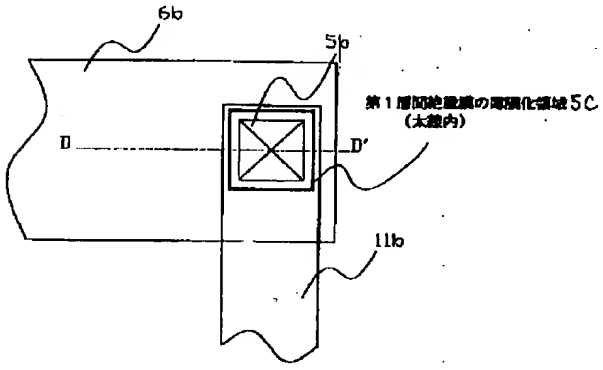
１２’…第１層間絶縁膜
１３…第２絶縁膜（第１層間絶縁膜の上層）
１９…配向膜
２０…対向基板
２１…対向電極
２２…配向膜
２３…遮光層
３０…ＴＦＴ
５０…液晶層
５２…シール材
５３…周辺見切り
７０…蓄積容量
１００…液晶装置
１０１…データ線駆動回路
１０４…走査線駆動回路

【図１】



＜画素平面図＞

【図２】



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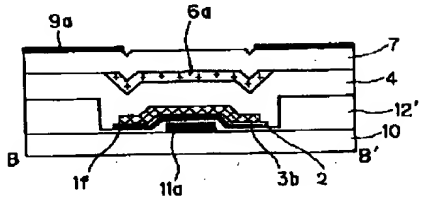

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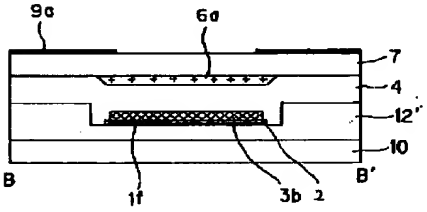
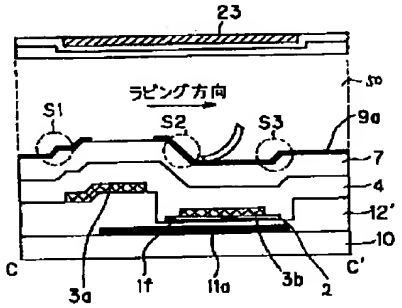
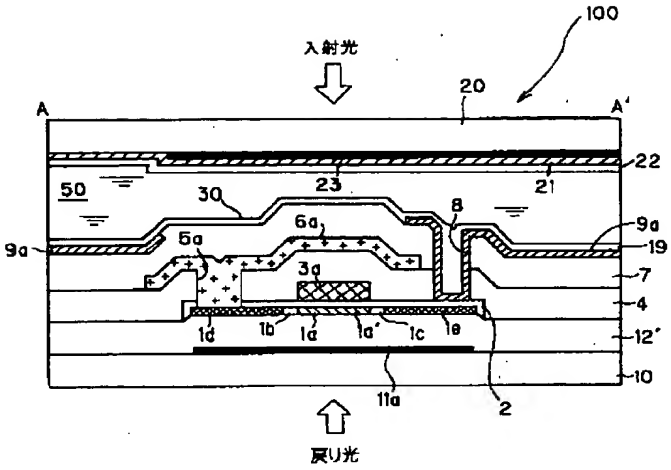


【図５】



【図３】



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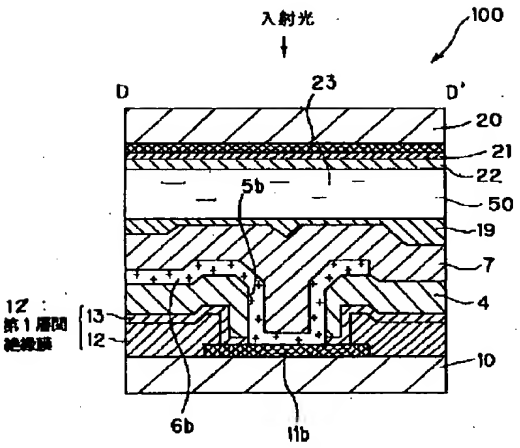
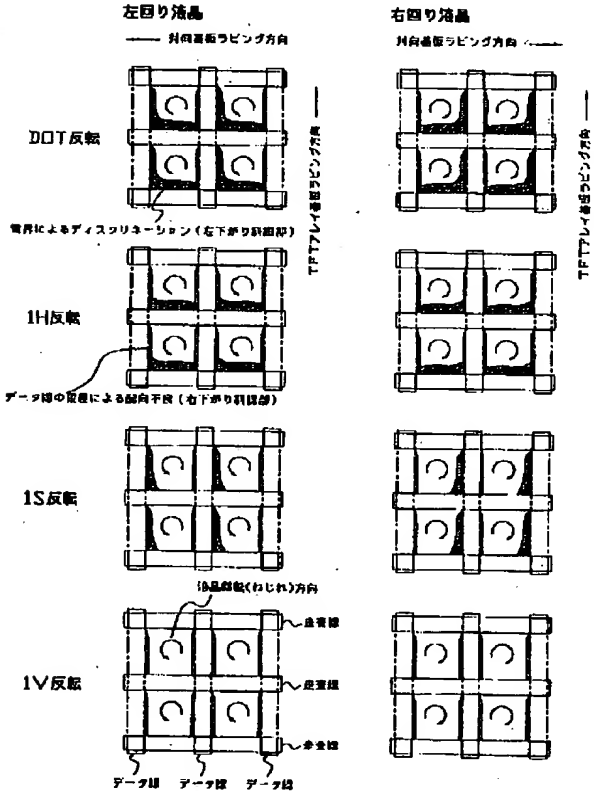


【図７】



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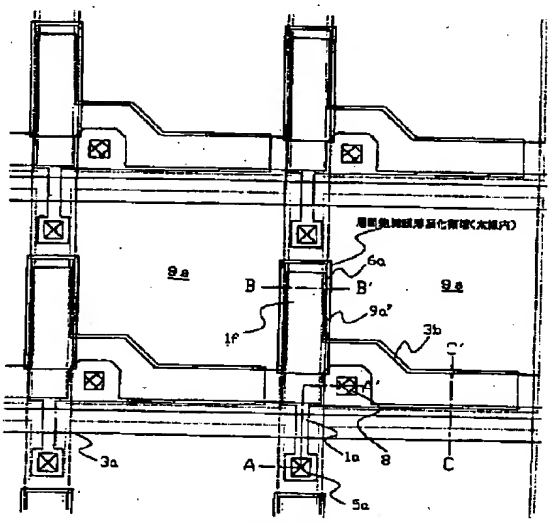
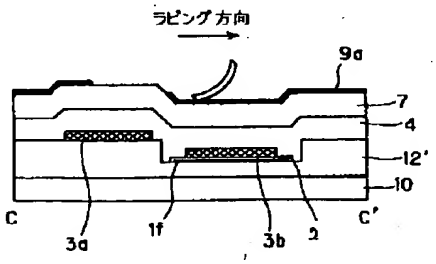


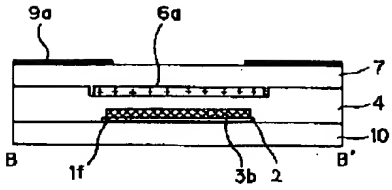
<画素平面図>

【図１０】



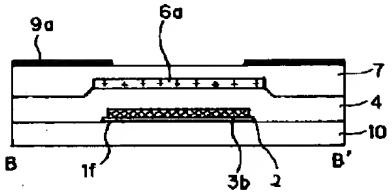
【図１１】

第2層間絶縁膜を薄膜化

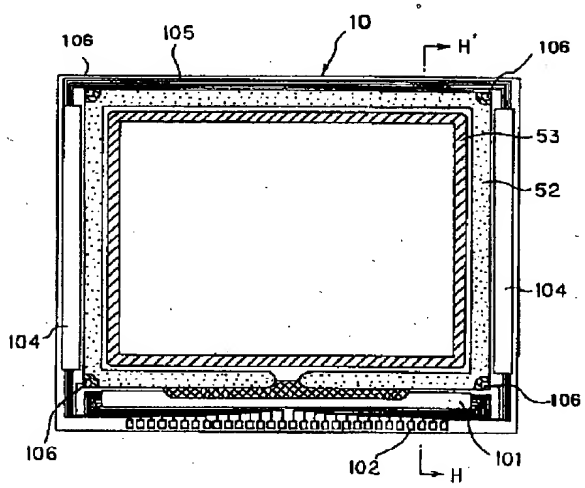


【図１２】

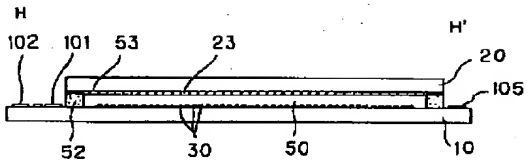
第3層間絶縁膜を薄膜化



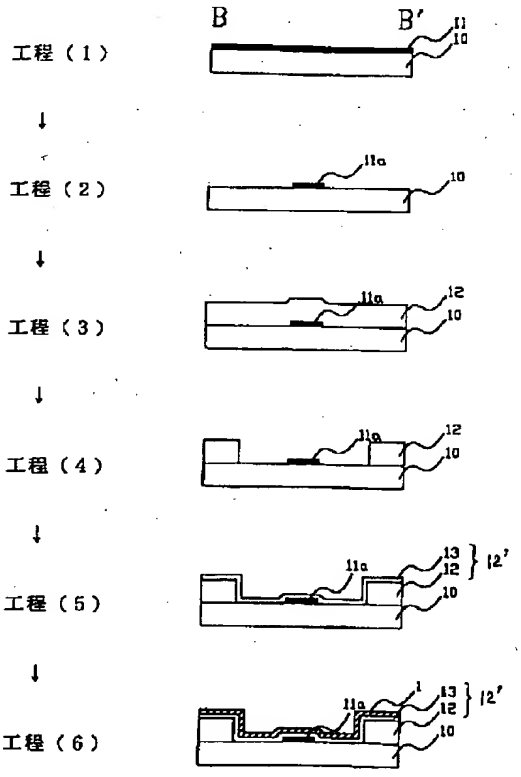
【図１３】



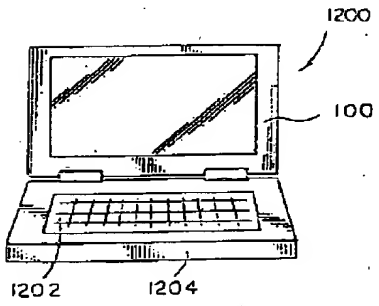
【図１４】



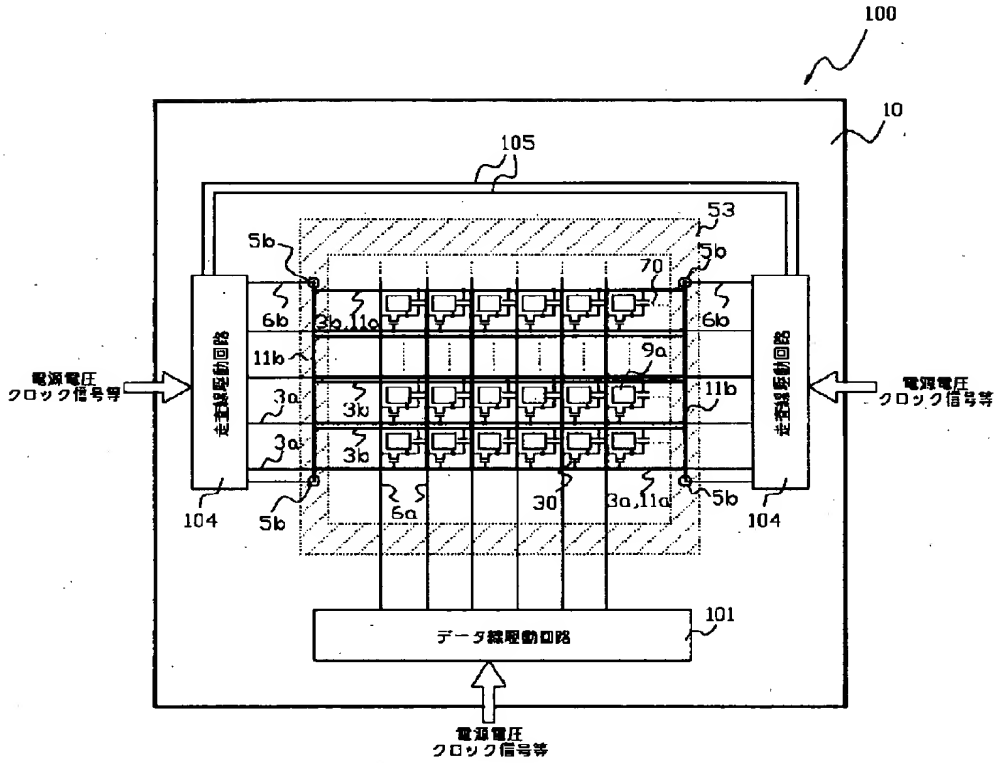
【図１６】



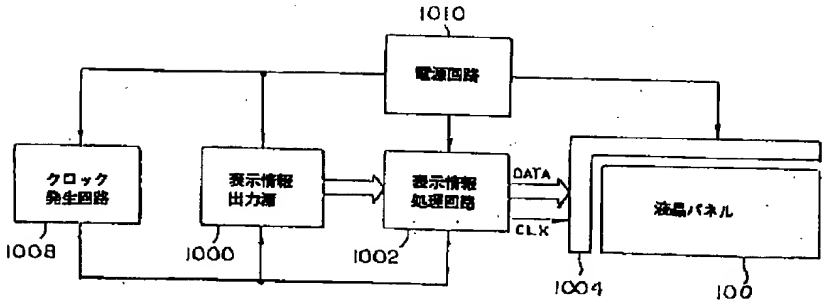
【図２６】



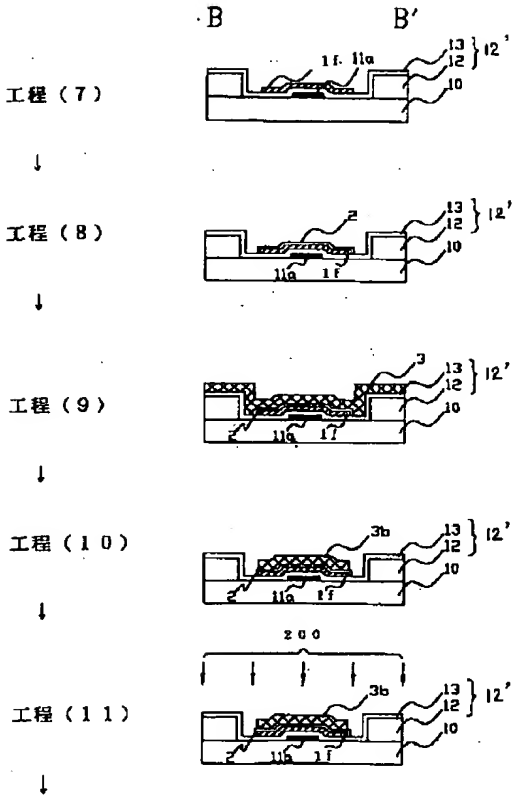
【図１５】


100
10
105
53
5b
70
6b
3b,11a
11b
9a
3a
3b
走査線駆動回路
電源電圧
クロック信号等
104
6a
30
データ線駆動回路
101

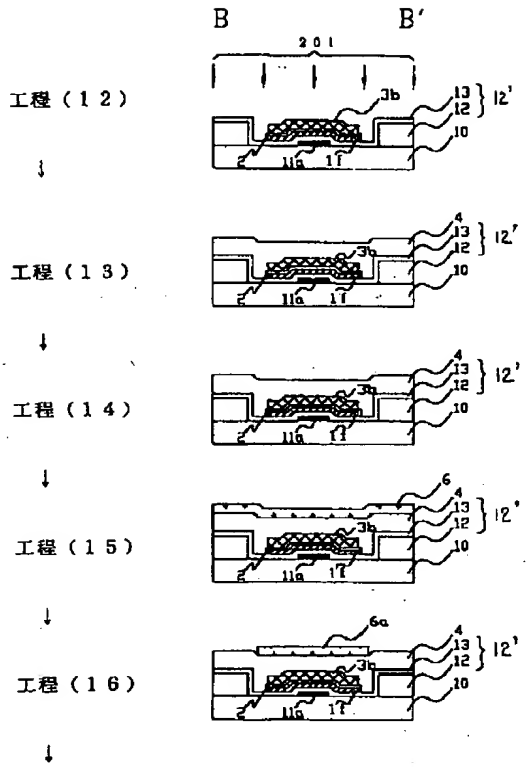
【図２４】


1010
電源回路
クロック
発生回路
表示情報
出力源
表示情報
処理回路
DATA
CLK
液晶パネル
1008
1000
1002
1004
100

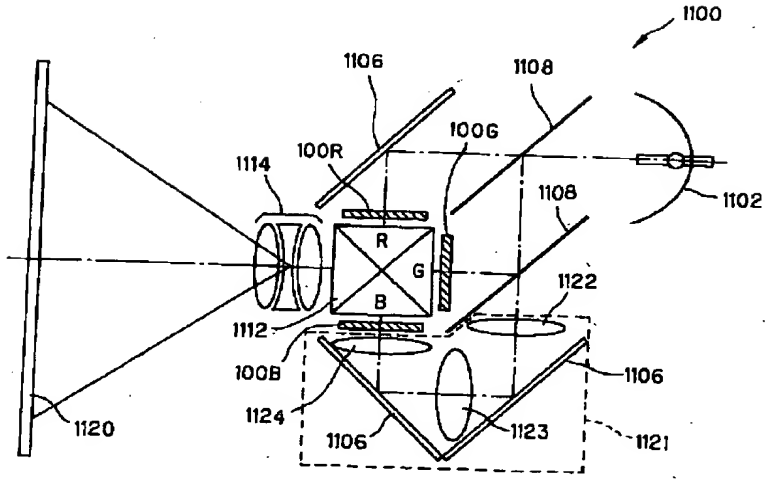
【図１７】


B
B′
工程（７）
工程（８）
工程（９）
工程（１０）
工程（１１）
200

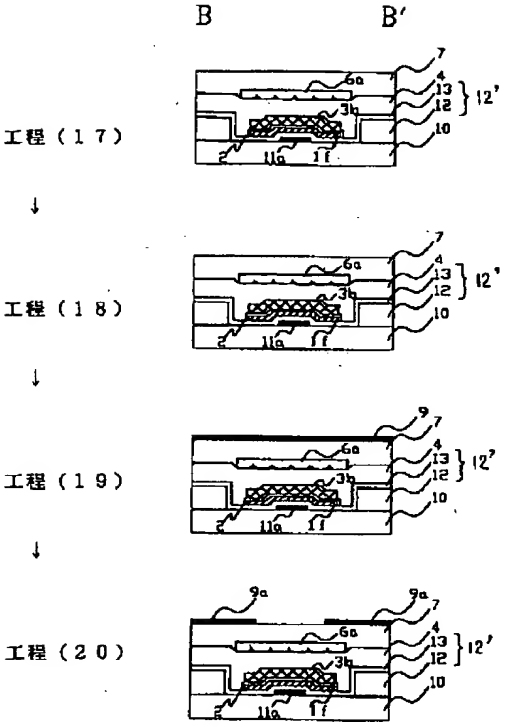
【図１８】


B
B′
工程（１２）
工程（１３）
工程（１４）
工程（１５）
工程（１６）
201

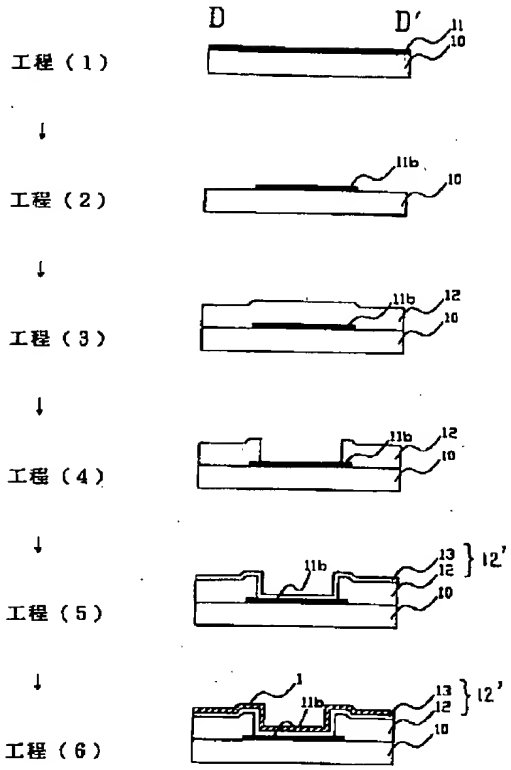
【図２５】


1100
1106
1108
1006
100R
1114
1102
R
G
B
1122
1112
100B
1124
1123
1121
1120

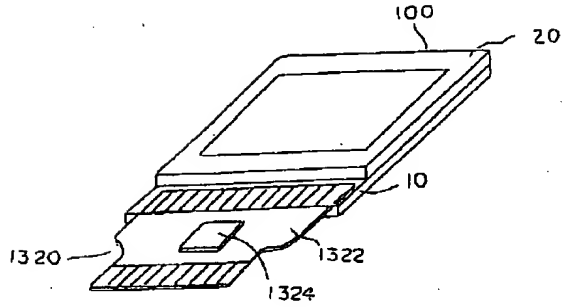
【図１９】


B
B'
工程（１７）
工程（１８）
工程（１９）
工程（２０）
7
4
13
12
12'
10
6a
3b
11a
11
9
9a

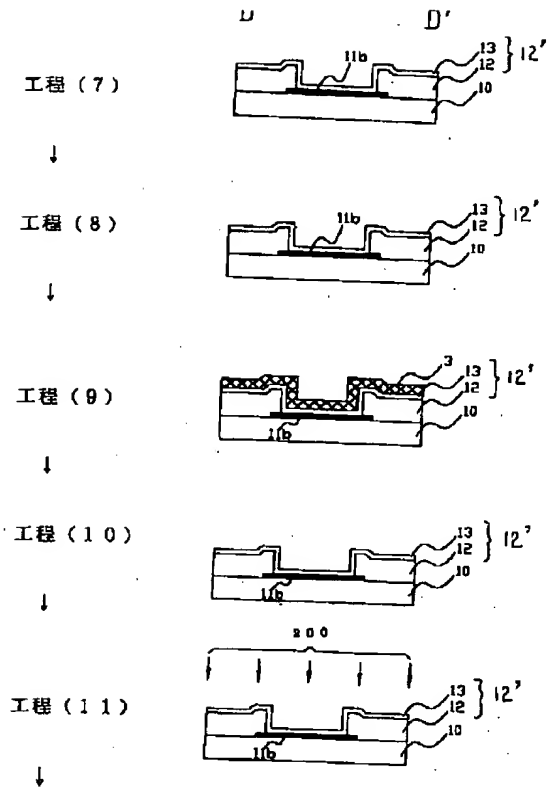
【図２０】


D
D'
工程（１）
工程（２）
工程（３）
工程（４）
工程（５）
工程（６）
11
10
11b
12
13
12'
1

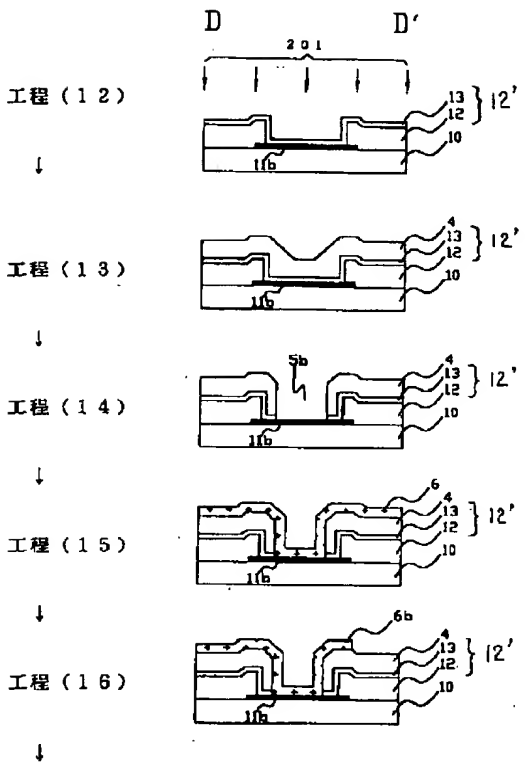
【図２８】


100
20
10
1320
1322
1324

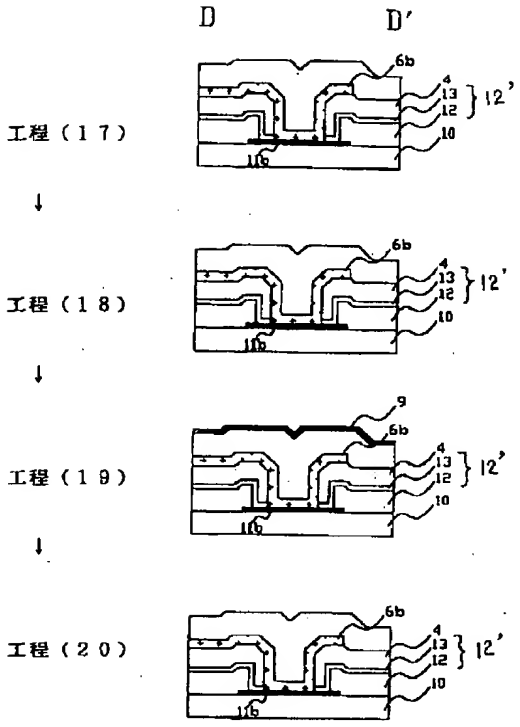
【図２１】


工程（７）
工程（８）
工程（９）
工程（１０）
工程（１１）
D
D'
11b
13
12
10
12'
3
200

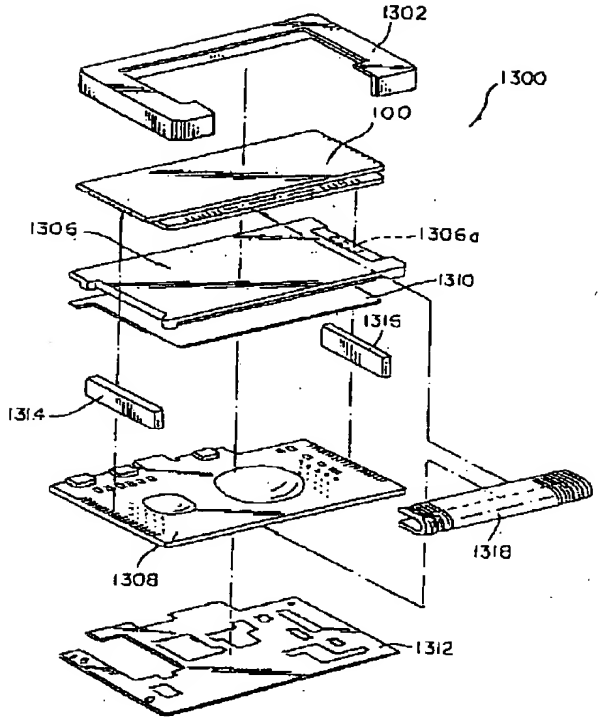
【図２２】


工程（１２）
工程（１３）
工程（１４）
工程（１５）
工程（１６）
D
D'
201
4
5b
6
6b
11b
13
12
10
12'

【図２３】


D
D'
工程（１７）
工程（１８）
工程（１９）
工程（２０）
6b
9
4
13
12
10
12'
116

【図２７】


1302
1300
100
1306
1306a
1310
1316
1314
1318
1308
1312

【公報種別】特許法第１７条の２の規定による補正の掲載
【部門区分】第６部門第２区分
【発行日】平成１４年４月１０日（２００２．４．１０）

【公開番号】特開平１１－２１８７８１
【公開日】平成１１年８月１０日（１９９９．８．１０）
【年通号数】公開特許公報１１－２１８８
【出願番号】特願平１０－２０００１
【国際特許分類第７版】
G02F　1/136　500
【ＦＩ】
G02F　1/136　500

【手続補正書】
【提出日】平成１３年１２月２０日（２００１．１２．２０）
【手続補正１】
【補正対象書類名】明細書
【補正対象項目名】特許請求の範囲
【補正方法】変更
【補正内容】
【特許請求の範囲】
【請求項１】一対の基板間に液晶が封入されてなり、該一対の基板の一方の基板上に複数のデータ線と、該複数のデータ線に交差する複数の走査線と、前記複数のデータ線及び走査線に各々接続された複数の薄膜トランジスタと、該複数の薄膜トランジスタに各々接続されて前記データ線より上方に配置された複数の画素電極と、該複数の薄膜トランジスタのドレイン又はソース領域を構成する半導体層と同一材料からなり少なくとも前記データ線下に各々延設された複数の第１蓄積容量電極部と、前記データ線下において前記複数の第１蓄積容量電極部と絶縁膜を介して各々対向配置された第２蓄積容量電極部を各々含む複数の容量線と、前記一方の基板と前記画素電極との間に配置された少なくとも１つの層間絶縁膜とを備えており、
前記層間絶縁膜は、前記容量線のうち少なくとも前記データ線下にある前記第２蓄積容量電極部に対向する領域が凹状に窪んで形成されてなることを特徴とする液晶装置。
【請求項２】　一対の基板間に液晶が封入されてなり、該一対の基板の一方の基板上に複数のデータ線と、該複数のデータ線に交差する複数の走査線と、前記複数のデータ線及び走査線に各々接続された複数の薄膜トランジスタと、該複数の薄膜トランジスタに各々接続された複数の画素電極と、該複数の薄膜トランジスタのドレイン又はソース領域を構成する半導体層と同一材料からなり少なくとも前記データ線下に各々延設された複数の第１蓄積容量電極部と、前記データ線下において前記複数の第１蓄積容量電極部と絶縁膜を介して各々対向配置された第２蓄積容量電極部を各々含む複数の容量線と、前記一方の基板及び前記第１蓄積容量電極部の間に配置されている第１層間絶縁膜と、前記第２蓄積容量電極部及び前記データ線の間に配置されている第２層間絶縁膜と、前記データ線及び前記画素電極の間に配置されている第３層間絶縁膜とを備えており、
前記第１、第２及び第３層間絶縁膜のうち少なくとも一つの絶縁膜は、前記容量線のうち少なくとも前記データ線下にある前記第２蓄積容量電極部に対向する領域が凹状に窪んで形成されたことを特徴とする液晶装置。
【請求項３】　前記複数の第１蓄積容量電極部は更に、前記複数の走査線と平行に各々延設されており、
前記複数の第２蓄積容量電極部は更に、前記走査線と平行に延設された前記第１蓄積容量電極部と前記容量形成用絶縁膜を介して対向配置されており、
前記少なくとも一つの絶縁膜は更に、前記容量線のうち前記走査線と平行な前記第２蓄積容量電極部に対向する領域が凹状に窪んで形成されたことを特徴とする請求項２に記載の液晶装置。
【請求項４】　前記画素電極上に配置されており、隣接して並べられた一対の走査線及び容量線に対して前記走査線の側から前記容量線の側に向う前記データ線に沿った方向でラビング処理された配向膜と、
前記一対の走査線及び容量線を前記走査線に沿った一本の帯部でまとめて覆う遮光層とを更に備えたことを特徴とする請求項３に記載の液晶装置。
【請求項５】　前記第１層間絶縁膜を前記一方の基板が兼ねており、前記第２及び第３層間絶縁膜のうち少なくとも一方は、前記容量線のうち少なくとも前記データ線下にある前記第２蓄積容量電極部に対向する領域が凹状に窪んで形成されたことを特徴とする請求項２から４のいずれか一項に記載の液晶装置。
【請求項６】　前記基板と前記第１層間絶縁膜との間において、前記複数の薄膜トランジスタの少なくともチャネル形成用領域を前記一方の基板の側から見て各々重なる位置に設けられた遮光膜を更に備えたことを特徴とす

る請求項２から５のいずれか一項に記載の液晶装置。
【請求項７】　前記遮光膜は、前記第１蓄積容量電極部の前記データ線下の部分及び前記走査線と平行な部分のうち少なくとも一方と前記第１層間絶縁膜を介して対向する位置に設けられた第３蓄積容量電極部を含んでおり、前記第１層間絶縁膜は、前記第３蓄積容量電極部と前記第１蓄積容量電極部との間の領域が前記凹状に窪んで形成されたことを特徴とする請求項６に記載の液晶装置。
【請求項８】　前記第１層間絶縁膜は、前記遮光膜は定電位源に接続されてなり、前記遮光膜と前記定電位源とが接続される位置において、前記凹状に窪んで形成されると共に開孔されたことを特徴とする請求項６又は７に記載の液晶装置。
【請求項９】　請求項５に記載の液晶装置の製造方法において、前記エッチング工程は、前記凹状に窪んだ部分の側壁をテーパ状に形成するウエットエッチング工程を含むことを特徴とする液晶装置の製造方法。
【請求項１０】　請求項６に記載の液晶装置の製造方法であって、前記走査線及び容量線を一対にして相隣接する前記画素電極間に並べるように前記第１層間絶縁膜上に形成する工程と、前記画素電極上及び前記画素電極が形成されていない前記第３層間絶縁膜の部分上に配向膜を形成する工程と、該配向膜を、前記一対の走査線及び容量線に対して前記走査線の側から前記容量線の側に向う前記データ線に沿った方向でラビング処理する工程とを備えたことを特徴とする液晶装置の製造方法。
【請求項１１】　請求項８に記載の液晶装置の製造方法であって、
前記一方の基板上の所定領域に前記遮光膜を形成する工程と、
前記接続される位置に対応する部分が前記凹状に窪むように前記一方の基板及び遮光膜上に前記第１層間絶縁膜を形成する工程と、
前記第１層間絶縁膜上に前記薄膜トランジスタを形成する工程と、
前記薄膜トランジスタ及び第１層間絶縁膜上に第２層間絶縁膜を形成する工程と、
前記遮光膜と前記定電位源からの配線とを接続するためのコンタクトホールとして、前記接続される位置において前記遮光膜に至るまで前記第２及び第１層間絶縁膜を開孔すると同時に、前記薄膜トランジスタと前記データ線とを接続するためのコンタクトホールとして、前記薄膜トランジスタを構成する半導体層のソース又はドレイン領域に対向する位置において前記半導体層に至るまで前記第２及び第１層間絶縁膜を開孔する工程と
を備えたことを特徴とする液晶装置の製造方法。
【請求項１２】　請求項１から１１に記載の液晶装置を備えたことを特徴とする電子機器。
【手続補正２】
【補正対象書類名】明細書
【補正対象項目名】００１０
【補正方法】変更
【補正内容】
【００１０】
【課題を解決するための手段】本発明は、上記課題を解決するために、一対の基板間に液晶が封入されてなり、該一対の基板の一方の基板上に複数のデータ線と、該複数のデータ線に交差する複数の走査線と、前記複数のデータ線及び走査線に各々接続された複数の薄膜トランジスタと、該複数の薄膜トランジスタに各々接続されて前記データ線より上方に配置された複数の画素電極と、該複数の薄膜トランジスタのドレイン又はソース領域を構成する半導体層と同一材料からなり少なくとも前記データ線下に各々延設された複数の第１蓄積容量電極部と、前記データ線下において前記複数の第１蓄積容量電極部と絶縁膜を介して各々対向配置された第２蓄積容量電極部を各々含む複数の容量線と、前記一方の基板と前記画素電極との間に配置された少なくとも１つの層間絶縁膜とを備えており、前記層間絶縁膜は、前記容量線のうち少なくとも前記データ線下にある前記第２蓄積容量電極部に対向する領域が凹状に窪んで形成されてなることを特徴とする。
【手続補正３】
【補正対象書類名】明細書
【補正対象項目名】００１１
【補正方法】変更
【補正内容】
【００１１】本発明によれば、第１蓄積容量電極部は、薄膜トランジスタのドレイン又はソース領域を構成する半導体層と同一材料からなり、少なくともデータ線下に各々延設されている。第２蓄積容量電極部は、少なくともデータ線下において第１蓄積容量電極部と絶縁膜を介して各々対向配置されている。このように本発明によれば、入射光が透過しないため開口領域としては使用不可能なデータ線下のスペースは、画素電極に対し容量を付与するためのスペースとして有効に使用されている。
【手続補正４】
【補正対象書類名】明細書
【補正対象項目名】００１２
【補正方法】変更
【補正内容】
【００１２】また、本発明によれば、層間絶縁膜は、容量線のうち少なくともデータ線下にある第２蓄積容量電極部に対向する領域が、他の領域と比べて凹状に窪んで形成されている。従って、データ線の上方に位置する画素電極面はこの窪みにより平坦化される。例えば、第１蓄積容量電極部、絶縁膜、第２蓄積容量電極部及びデータ線の合計層厚に等しい深さだけ凹状に窪めれば、画素電極面は、ほぼ完全に平坦化される。

【手続補正５】
【補正対象書類名】明細書
【補正対象項目名】００１３
【補正方法】変更
【補正内容】
【００１３】以上のように従来は、段差によりラビング処理が適切に施せなかったことに起因して、或いは段差による基板間距離の狂いに直接起因して液晶の配向不良は、この開口領域のデータ線に沿った部分で最も起き易かったが、本発明によれば、この部分における配向不良を平坦化により低減できる。
【手続補正６】
【補正対象書類名】明細書
【補正対象項目名】００１４
【補正方法】変更
【補正内容】
【００１４】さらに、本発明は、一対の基板間に液晶が封入されてなり、該一対の基板の一方の基板上に複数のデータ線と、該複数のデータ線に交差する複数の走査線と、前記複数のデータ線及び走査線に各々接続された複数の薄膜トランジスタと、該複数の薄膜トランジスタに各々接続された複数の画素電極と、該複数の薄膜トランジスタのドレイン又はソース領域を構成する半導体層と同一材料からなり少なくとも前記データ線下に各々延設された複数の第１蓄積容量電極部と、前記データ線下において前記複数の第１蓄積容量電極部と絶縁膜を介して各々対向配置された第２蓄積容量電極部を各々含む複数の容量線と、前記一方の基板及び前記第１蓄積容量電極部の間に配置されている第１層間絶縁膜と、前記第２蓄積容量電極部及び前記データ線の間に配置されている第２層間絶縁膜と、前記データ線及び前記画素電極の間に配置されている第３層間絶縁膜とを備えており、前記第１、第２及び第３層間絶縁膜のうち少なくとも一つの絶縁膜は、前記容量線のうち少なくとも前記データ線下にある前記第２蓄積容量電極部に対向する領域が凹状に窪んで形成されたことを特徴とする。
【手続補正７】
【補正対象書類名】明細書
【補正対象項目名】００１５
【補正方法】変更
【補正内容】
【００１５】本発明によれば、第１蓄積容量電極部は、薄膜トランジスタのドレイン又はソース領域を構成する半導体層と同一材料からなり、少なくともデータ線下に各々延設されている。第２蓄積容量電極部は、少なくともデータ線下において第１蓄積容量電極部と絶縁膜を介して各々対向配置されている。このように本発明によれば、入射光が透過しないため開口領域としては使用不可能なデータ線下のスペースは、画素電極に対し容量を付与するためのスペースとして有効に使用されている。
【手続補正８】
【補正対象書類名】明細書
【補正対象項目名】００１８
【補正方法】変更
【補正内容】
【００１８】本発明の液晶装置は上記課題を解決するために前記複数の第１蓄積容量電極部は更に、前記複数の走査線と平行に各々延設されており、前記複数の第２蓄積容量電極部は更に、前記走査線と平行に延設された前記第１蓄積容量電極部と前記容量形成用絶縁膜を介して対向配置されており、前記少なくとも一つの絶縁膜は更に、前記容量線のうち前記走査線と平行な前記第２蓄積容量電極部に対向する領域が凹状に窪んで形成されたことを特徴とする。
【手続補正９】
【補正対象書類名】明細書
【補正対象項目名】００１９
【補正方法】変更
【補正内容】
【００１９】この発明によれば、第１蓄積容量電極部と第２蓄積容量電極部とは、走査線と平行な領域において、容量形成用絶縁膜を介して対向配置されている。このように本発明によれば、データ線下だけでなく、走査線に平行な領域も、画素電極に対し容量を付与するためのスペースとして有効に使用されている。ここで一般に、走査線に平行に容量線が配線される領域は、開口領域内に位置する画素部と比較すると、第１蓄積容量電極部、容量形成用絶縁膜及び第２蓄積容量電極部が積層されている分だけ段差ができる。しかるに、本発明によれば、第１、第２及び第３層間絶縁膜のうち少なくとも一つの絶縁膜は、容量線のうち少なくとも走査線と平行な第２蓄積容量電極部に対向する領域が、凹状に窪んで形成されている。従って、この容量線の上方に位置する第３層間絶縁膜の上面或いはこの上に形成される画素電極面は、この窪みに応じて平坦化される。例えば、第１蓄積容量電極部、容量形成用絶縁膜及び第２蓄積容量電極部の合計層厚に等しい深さだけ凹状に窪めれば、第３層間絶縁膜の上面或いはこの上に形成される画素電極面は、ほぼ完全に平坦化される。
【手続補正１０】
【補正対象書類名】明細書
【補正対象項目名】００２０
【補正方法】変更
【補正内容】
【００２０】本発明の液晶装置は前記画素電極上に配置されており、隣接して並べられた一対の走査線及び容量線に対して前記走査線の側から前記容量線の側に向う前記データ線に沿った方向でラビング処理された配向膜と、前記一対の走査線及び容量線を前記走査線に沿った一本の帯部でまとめて覆う遮光層とを更に備えたことを

特徴とする。
【手続補正１１】
【補正対象書類名】明細書
【補正対象項目名】００２１
【補正方法】変更
【補正内容】
【００２１】この発明によれば、ＴＦＴアレイ基板において配向膜は、画素電極上に配置されており、隣接して並べられた一対の走査線及び容量線に対して走査線の側から容量線の側に向うデータ線に沿った方向でラビング処理されている。ここで一般に、ラビング方向に面が高くなる段差に対してはラビング処理は比較的良好に行われ、ラビング方向に面が低くなる段差に対してはラビング処理は良好に行うことが困難であることが本発明者による研究の結果判明している。そこで、本発明のように、平坦化を施していない走査線の側から平坦化を施した容量線の側に向けた方向でラビング処理を行うようにすれば、ラビング方向の上流に位置する画素側の走査線の一方の縁における段差は、ラビング方向に面が高くなる段差となるのでラビング処理が良好に行われる。他方、容量線に隣接する側の走査線の他方の縁における段差は、ラビング方向に面が低くなる段差となるのでラビング処理が良好に行われない。しかしながら、この部分とラビング方向の下流に位置する画素との間には容量線の上方に位置する平坦化された面があると共に、遮光層の一本の帯部により、まとめて覆われているので開口領域から遠く離れている。このため、走査線の他方の縁に対応してラビング処理が良好に行われなくても、これによる液晶の配向不良が画像に影響することは殆ど又は全く無い。仮に、ラビング処理の方向を反対にしてしまうと、ラビング方向に面が低くなる段差が、容量線から遠い方の走査線の縁に現われてしまい、これによる液晶の配向不良が画像に影響を及ぼしてしまうか或いは、このような部分を更に遮光層で覆うことにより開口領域を狭めねばならない。
【手続補正１２】
【補正対象書類名】明細書
【補正対象項目名】００２３
【補正方法】削除
【手続補正１３】
【補正対象書類名】明細書
【補正対象項目名】００２４
【補正方法】削除
【手続補正１４】
【補正対象書類名】明細書
【補正対象項目名】００２５
【補正方法】削除
【手続補正１５】
【補正対象書類名】明細書
【補正対象項目名】００２６
【補正方法】削除
【手続補正１６】
【補正対象書類名】明細書
【補正対象項目名】００２７
【補正方法】削除
【手続補正１７】
【補正対象書類名】明細書
【補正対象項目名】００２８
【補正方法】削除
【手続補正１８】
【補正対象書類名】明細書
【補正対象項目名】００２９
【補正方法】変更
【補正内容】
【００２９】請本発明の液晶装置において、前記第１層間絶縁膜を前記一方の基板が兼ねており、前記第２及び第３層間絶縁膜のうち少なくとも一方は、前記容量線のうち少なくとも前記データ線下にある前記第２蓄積容量電極部に対向する領域が凹状に窪んで形成されたことを特徴とする。
【手続補正１９】
【補正対象書類名】明細書
【補正対象項目名】００３０
【補正方法】変更
【補正内容】
【００３０】この発明によれば、一方の基板が第１層間絶縁膜を兼ねている。即ち、一方の基板がＴＦＴの下地膜としても機能し、第１層間絶縁膜は省略される。しかるに、本発明によれば、第２及び第３層間絶縁膜のうち少なくとも一方は、容量線のうち少なくともデータ線下にある第２蓄積容量電極部に対向する領域が凹状に窪んで形成されているので、上述の本発明と同様に第３層間絶縁膜の上面や画素電極面の平坦化が図られる。
【手続補正２０】
【補正対象書類名】明細書
【補正対象項目名】００３１
【補正方法】変更
【補正内容】
【００３１】本発明は、前記基板と前記第１層間絶縁膜との間において、前記複数の薄膜トランジスタの少なくともチャネル形成用領域を前記一方の基板の側から見て各々重なる位置に設けられた遮光膜を更に備えたことを特徴とする。
【手続補正２１】
【補正対象書類名】明細書
【補正対象項目名】００３２
【補正方法】変更
【補正内容】
【００３２】この発明によれば、遮光膜は、複数のＴＦＴの少なくともチャネル形成用領域を一方の基板の側か

ら見て各々重なる位置において一方の基板に設けられている。従って、一方の基板の側からの戻り光等が当該チャネル形成用領域に入射する事態を未然に防ぐことができ、光電流の発生によりＴＦＴの特性が劣化することはない。そして、遮光膜は、一方の基板と第１層間絶縁膜との間に設けられている。従って、遮光膜からＴＦＴ等を電気的絶縁し得ると共に遮光膜がＴＦＴ等を汚染する事態を未然に防げる。

【手続補正２２】
【補正対象書類名】明細書
【補正対象項目名】００３３
【補正方法】変更
【補正内容】
【００３３】本発明は、前記遮光膜は、前記第１蓄積容量電極部の前記データ線下の部分及び前記走査線と平行な部分のうち少なくとも一方と前記第１層間絶縁膜を介して対向する位置に設けられた第３蓄積容量電極部を含んでおり、前記第１層間絶縁膜は、前記第３蓄積容量電極部と前記第１蓄積容量電極部との間の領域が前記凹状に窪んで形成されたことを特徴とする。

【手続補正２３】
【補正対象書類名】明細書
【補正対象項目名】００３４
【補正方法】変更
【補正内容】
【００３４】この発明によれば、遮光膜は、第１蓄積容量電極部のデータ線下の部分及び走査線と平行な部分のうち少なくとも一方と第１層間絶縁膜を介して対向する位置に設けられた第３蓄積容量電極部を含んでいる。従って、容量形成用絶縁膜を介して対向配置された第１蓄積容量電極部と第２蓄積容量電極部とで形成される容量に加えて、第１層間絶縁膜を介して対向配置された第１蓄積容量電極部と第３蓄積容量電極部とで形成される容量も、蓄積容量として画素電極に付与される。ここで一般に、容量形成用に間に介在する絶縁膜の膜厚が厚いほど形成される容量は小さく、薄いほど形成される容量は大きくなる。しかるに、本発明によれば、第１層間絶縁膜は、第３蓄積容量電極部と第１蓄積容量電極部との間の領域が凹状に窪んで形成されているため、容量形成用に間に介在する絶縁膜の膜厚を凹状の窪みの深さに応じて薄くすることが出来る。この結果、第１及び第３蓄積容量電極部の表面積を増やすことなく容量を効率的に増やすことが出来る。

【手続補正２４】
【補正対象書類名】明細書
【補正対象項目名】００３５
【補正方法】削除
【手続補正２５】
【補正対象書類名】明細書
【補正対象項目名】００３６
【補正方法】削除
【手続補正２６】
【補正対象書類名】明細書
【補正対象項目名】００３７
【補正方法】削除
【手続補正２７】
【補正対象書類名】明細書
【補正対象項目名】００３８
【補正方法】削除
【手続補正２８】
【補正対象書類名】明細書
【補正対象項目名】００３９
【補正方法】変更
【補正内容】
【００３９】本発明は、前記第１層間絶縁膜は、前記遮光膜は定電位源に接続されてなり、前記遮光膜と前記定電位源とが接続される位置において、前記凹状に窪んで形成されると共に開孔されたことを特徴とする。

【手続補正２９】
【補正対象書類名】明細書
【補正対象項目名】００４０
【補正方法】変更
【補正内容】
【００４０】この本発明によれば、第１層間絶縁膜は、遮光膜と定電位源とが接続される位置において凹状に窪んで形成されているので、その製造プロセスにおいて、当該第１層間絶縁膜形成後に、この凹状に窪んだ部分の深さに応じて、この位置を開孔する工程が容易となる。

【手続補正３０】
【補正対象書類名】明細書
【補正対象項目名】００４１
【補正方法】削除
【手続補正３１】
【補正対象書類名】明細書
【補正対象項目名】００４２
【補正方法】削除
【手続補正３２】
【補正対象書類名】明細書
【補正対象項目名】００４３
【補正方法】削除
【手続補正３３】
【補正対象書類名】明細書
【補正対象項目名】００４４
【補正方法】削除
【手続補正３４】
【補正対象書類名】明細書
【補正対象項目名】００４５
【補正方法】変更
【補正内容】
【００４５】本発明の液晶装置の製造方法であって、前

記エッチング工程は、少なくとも前記凹状に窪んだ部分の側壁をテーパ状に形成するウエットエッチング工程を含むことを特徴とする。

【手続補正３５】
【補正対象書類名】明細書
【補正対象項目名】００４６
【補正方法】変更
【補正内容】
【００４６】この発明によれば、ウエットエッチング工程により、凹状に窪んだ部分の側壁は、テーパ状に形成される。このように凹状に窪んだ部分の側壁をテーパ状に形成しておけば、凹状に窪んだ部分内に後工程で形成される、例えば、ポリシリコン膜等が残ることがない。このため、この部分を確実に平坦化できる。また、ドライエッチングとウエットエッチングとを組み合わせてもよいことは言うまでもない。

【手続補正３６】
【補正対象書類名】明細書
【補正対象項目名】００４７
【補正方法】変更
【補正内容】
【００４７】本発明の液晶装置の製造方法は上記課題を解決するために前記走査線及び容量線を一対にして相隣接する前記画素電極間に並べるように前記第１層間絶縁膜上に形成する工程と、前記画素電極上及び前記画素電極が形成されていない前記第３層間絶縁膜の部分上に配向膜を形成する工程と、該配向膜を、前記一対の走査線及び容量線に対して前記走査線の側から前記容量線の側に向う前記データ線に沿った方向でラビング処理する工程とを備えたことを特徴とする。

【手続補正３７】
【補正対象書類名】明細書
【補正対象項目名】００４８
【補正方法】変更
【補正内容】
【００４８】この発明によれば、一対の走査線及び容量線は相隣接する画素電極間に並ぶように、走査線及び容量線は第１層間絶縁膜上に形成される。次に、画素電極上及び画素電極が形成されていない第３層間絶縁膜の部分上に、配向膜を形成される。そして次に、該配向膜は、一対の走査線及び容量線に対して走査線の側から容量線の側に向うデータ線に沿った方向で、ラビング処理される。従って前述のように、ラビング方向の上流に位置する走査線のラビング処理が良好に行われない縁は開口領域から離れているので、この縁付近における液晶の配向不良が画像に影響することは殆ど又は全く無い。特に前述のように走査線反転駆動方式を用いる際には高コントラスト化と高精細化を図る上で、大変有利である。

【手続補正３８】
【補正対象書類名】明細書
【補正対象項目名】００４９
【補正方法】変更
【補正内容】
【００４９】本発明は、前記一方の基板上の所定領域に前記遮光膜を形成する工程と、前記接続される位置に対応する部分が前記凹状に窪むように前記一方の基板及び遮光膜上に前記第１層間絶縁膜を形成する工程と、前記第１層間絶縁膜上に前記ＴＦＴを形成する工程と、前記ＴＦＴ及び第１層間絶縁膜上に第２層間絶縁膜を形成する工程と、前記遮光膜と前記定電位源からの配線とを接続するためのコンタクトホールとして、前記接続される位置において前記遮光膜に至るまで前記第２及び第１層間絶縁膜を開孔すると同時に、前記ＴＦＴと前記データ線とを接続するためのコンタクトホールとして、前記ＴＦＴを構成する半導体層のソース又はドレイン領域に対向する位置において前記半導体層に至るまで前記第２層間絶縁膜を開孔する工程とを備えたことを特徴とする。

【手続補正３９】
【補正対象書類名】明細書
【補正対象項目名】００５０
【補正方法】変更
【補正内容】
【００５０】この発明によれば、一方の基板上の所定領域に遮光膜が形成され、遮光膜と定電位源とが接続される位置に対応する部分が凹状に窪むように一方の基板及びこの遮光膜上に第１層間絶縁膜が形成される。その後、ＴＦＴが第１層間絶縁膜上に形成され、更にＴＦＴ及び第１層間絶縁膜上に第２層間絶縁膜が形成される。この第２層間絶縁膜は、ＴＦＴ、データ線、走査線、容量線等の電気絶縁用に設けられるものである。ここで、遮光膜と定電位源からの配線とを接続するためのコンタクトホールとして、遮光膜に至るまで第２及び第１層間絶縁膜が開孔され、同時に、ＴＦＴとデータ線とを接続するためのコンタクトホールとして、半導体層に至るまで第２層間絶縁膜が開孔される。従って、これら２種類のコンタクトホールを一括して開孔できる。

【手続補正４０】
【補正対象書類名】明細書
【補正対象項目名】００５１
【補正方法】変更
【補正内容】
【００５１】本発明は、上記に記載の液晶装置を備えたことを特徴とする。

【手続補正４１】
【補正対象書類名】明細書
【補正対象項目名】００５２
【補正方法】変更
【補正内容】
【００５２】この発明によれば、電子機器は、上述した本願発明の液晶装置を備えており、平坦化された画素電

極により液晶の配向不良の少ない液晶装置により高品位の画像表示が可能となる。